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Research article

TI-ADC multi-channel mismatch estimation and calibration in ultra-high-speed optical signal acquisition system

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Abstract: This article presents a method to calibrate a 16-channel 40 GS/s time-interleaved analog-to-digital converter (TI-ADC) based on channel equalization and Monte Carlo method. First, the channel mismatch is estimated by the Monte Carlo method, and equalize each channel to meet the calibration requirement. This method does not require additional hardware circuits, every channel can be compensated. The calibration structure is simple and the convergence speed is fast, besides, the ADC is worked in background mode, which does not affect the conversion. The prototype, implemented in 28 nm CMOS, reaches a 41 dB SFDR with an input signal of 1.2 GHz and 5 dBm after the proposed background offset and gain mismatch calibration. Compared with previous works, the spurious-free dynamic range (SFDR) and the effective number of bits (ENOB) are better, the estimation accuracy is higher, the error is smaller and the faster speed of convergence improves the efficiency of signal processing.

Keywords: analog-to-digital conversion; Monte Carlo estimation; channel equalization; field programmable gate array (FPGA)

1. Introduction

With the popularization of Internet, various new media promote the explosive development of the network industry. The transmission bandwidth requirements of metropolitan area networks and backbone networks continue to increase. Reference [1] proposes a method which includes two pilot scheduling schemes, fractional pilot reuse (FPR) and asynchronous fractional pilot scheduling (AFPS) scheme, which significantly mitigate the personal computer (PC) in the uplink time division duplex

(TDD) massive multiple-input-multiple-output (MIMO) system. Reference [2] describes a machine learning and deep learning concepts in optical 5G network, they collect the data first, and operate the optimal weighted feature extraction (OWFE), then they finish the slicing classification. Their model can influence the provision of accurate 5G network slicing. In 5G communication and MIMO system, there are still many challenges to the deployment of transmission systems. In order to transfer the photoelectric conversion analog signals into the digital domain, ADC plays an important role.

The traditional intermediate frequency (IF) signal acquisition platform is shown in Figure 1. With the help of a software radio structure, the microwave signal received by the antenna is mixed, converted into an IF signal, and then it is sampled after the signal conditioning links such as amplification and filtering; however, for the 20 Gbps radio frequency signal, the IF method cannot directly sample the radio frequency signal, so the radio frequency (RF) signal sampling structure is created, which is shown in Figure 1. First, it receives the radio frequency signal, and passes through a filter to reduce noise. After filtering through a low noise amplifier (LNA), it enters the ADC to achieve analog-to-digital conversion. Compared with the traditional sampling method, the structure is simpler and it is more suitable for high-bandwidth signals.

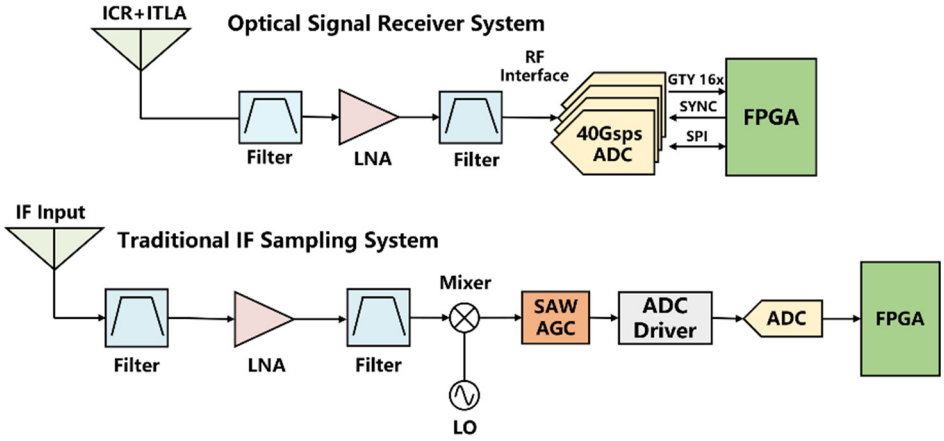


Figure 1. RF sampling compared with traditional IF sampling.

In order to meet the requirements of RF signal sampling frequency, the sampling method of multi-channel time interleaving is proposed and widely used in ultra-wideband communication and high-speed serial communication. The structure and clock phase are shown in Figure 2, M channels sample alternately, and the sampling frequency becomes M times that of a single channel. Although the time interleaved technology increases the sampling frequency on the limited hardware resources, due to process issues and device aging, stress imbalance and temperature drift, etc., the gain, offset and delay of each channel will be randomly distributed (gain and offset are the values by which the input values are multiplied and then to which the input values are added, respectively), and such errors will be amplified several times under the influence of high speed, which seriously affect the accuracy of ADC, so ADC calibration becomes a key step in the process of digital signal.

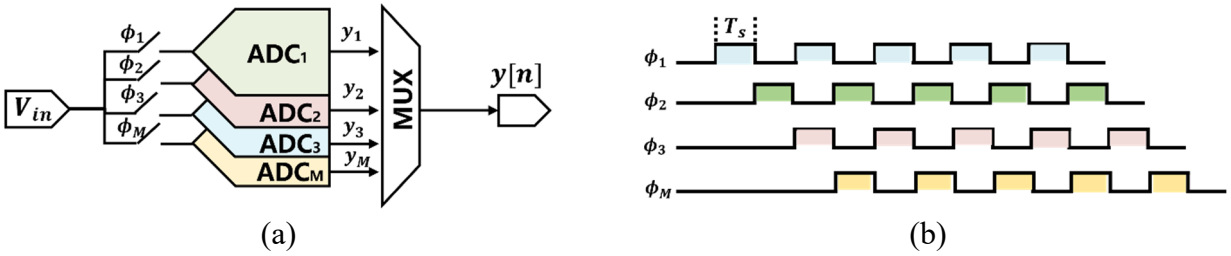


Figure 2. (a) M-channel TI ADC; (b) Its clock phase.

In recent years, scholars have mostly used equalization technology, adaptive blind correction, and random chopping sampling technology for calibrating the channel mismatch. Some works propose inter-channel equalization technology to solve the gain mismatch [3–6], they divide the convergence process into several phases and assist with a monotonicity detector to decide when to shift from one phase to the next phase. Selecting one of the channels as the reference channel will cause the channel to fail to perform self-calibration, and the calibration model lacks completeness, secondly, the addition of the reference channel makes the input impedance change, which is an obvious shortcoming for ultra-high-speed ADCs. The method proposed in [7] is to estimate the mismatch between channels, the technique is based on the discrete Fourier transform (DFT) for estimating and correcting gain mismatch and timing error in an M-ADC, which also describes the influence of these mismatches, however, the research does not propose a method to compensate the offset error, the technique is lack of integrity. In [8], an fast Fourier transform (FFT)-based method to evaluate and compensate offset and gain errors in time-interleaved ADC system is proposed with a known sinusoidal input. In [9], a digital background calibration method is proposed to calibrate the offset and gain mismatch as well as the timing error.

Reference [10] proposes a digital hybrid background calibration for time delay, with a 5 GS/s 29 mW TI successive-approximation-register (SAR) ADC, and the calibrated signal noise distortion rate (SNDR) reaches 48.5 dB (which is also called signal-to-noise-and-distortion ratio (SINAD) officially in the IEEE Standard, in order not to confuse the two definitions (SNDR and SINAD) later in the text, the subsequent exposition is consistent with the standard and is referred to as SINAD). They use a model of parameter mixed between channels, and estimate the time delay based on Nyquist frequency, the method is divided into 4 steps to achieve channel alignment. Finally, the calibration is completed in the order of offset and gain. However, the reason for the offset and gain mismatch is attributed to the delay in the article, after estimation and compensation, the offset and gain mismatch are resolved. For ultra-high-speed optical signal acquisition systems, the sources of mismatch are more complicated, and the effects of offset and gain need to be considered separately on the basis of completing channel alignment. Reference [11] divides the TI structure into two topological structures, which improves the convergence speed of time offset calibration, and SINAD can reach 54.2 dB; Reference [12] mainly introduces the calibration of bandwidth mismatch, based on the traditional method, constructs a kind of FIR filter to implement signal compensation. References [9] and [13] describe an algorithm for evaluating ADC performance, and comprehensively analyzes the impact of bandwidth mismatch on sampling. References [14,15] are different from the traditional background calibration, the calibration method of the digital-to-analog converter (DAC) in the feedback link is introduced, which further improves the calibration effect. References [16–18] analyze the influence of channel mismatch

sampling, they use the channel cross feedback mechanism to equalize the mismatch, and design a peripheral delay circuit to compensate for the offset of the calibration clock, which eliminate the energy of harmonics, and improve SINAD; References [19–22] propose a background calibration method that does not require pre-emphasis based on a 65 nm, 6-bit, 16 GS/s TI ADC. The offset mismatch is reduced after digital calibration, the delay phase locked loop is used to generate 8 sampling interfaces as multi-phase clock generator; References [23–25] propose a blind method to estimate channel mismatch and timing skew, this method does not need to know the input signal, as long as it meets the required bandwidth, calibration can be done while ADC is converting, it can be applied to many environments. The above works are all carried out around the background calibration. Compared with the foreground calibration, the background calibration can better monitor the power and temperature of the system, besides, it will not affect the normal sampling of the ADC. 1241–2010 IEEE Standard in [26] provides the standard for terminology and test methods for analog-to-digital converters, which also includes the method to calculate the gain and offset mismatch.

Different from the previous research works, this article does not select an actual channel as the reference channel, which means all channels can be calibrated and there is no impedance mismatch. When every channel meets the standard (offset and gain error are 0), the calibration is completed, otherwise, calibrate it until convergence. We estimate the mismatch first and design a channel equalization structure to calibrate, such method can reduce the error and the signal quality is further improved. Besides, there are a variety of random noise in the complex transmission channel, traditional methods are not stable especially at a high sampling frequency, however, Monte Carlo method happens to be flexible to deal with these random issues, so the relative error of estimation is smaller and reduces the number of iterations. After calibration, the SFDR reaches 41.72 dB and the SINAD increases from 21.65 dB to 30.16 dB, the signal-to-noise ratio (SNR) improves from 21.91 dB to 30.58 dB and ENOB achieves 5.76 bits, such method shows a better performance than other methods in the same experiment condition.

The rest of this article is organized as follows: Section 2 describes the impact of mismatch on ADC. Section 3 reviews the accumulative average algorithm used in the channel equalization process. Section 4 describes the improvement of the channel equalization algorithm. Section 5 is the hardware implementation and experiment results compared with other art works. Section 6 draws the conclusion.

2. The influence of mismatch

There are two versions to define the gain and offset: 1) (independently based) gain and offset are the values by which the input values are multiplied and then to which the input values are added, respectively, to minimize the mean squared deviation from the output values. 2) (terminal based) gain and offset are the values by which the input values are multiplied and then to which the input values are added, respectively, to cause the deviations from the output values to be zero at the terminal points, that is, at the first and last codes. In order to verify the derivation, we simulate the mismatch by a 4-channel 8-bit ADC with the sampling frequency at 40 GS/s, there are two types of input signals: the input frequency f_{in} is 1.2 GHz and 12 GHz, both voltage of the input signal is 1 V.

2.1. Analysis of offset mismatch

Because the processing is performed in the digital domain, the processing process is based on the binary output, the input of the circuit is a standard sinusoidal signal, therefore, in the complete cycle, the average value of the output code is 0, compared the actual average value with 0 can get the offset mismatch. The same input voltage, output different codes, subtracting a calibrated offset mismatch from this code is the output result after calibration. The conversion structure is shown in Figure 3(a), each channel has an offset mismatch O_i [27], the mismatch cause the transfer curve to deviate from the ideal curve, as shown in Figure 3(b). At the same time, the temperature drift and stress of the chip will also affect it. A certain range of fluctuations are generated on the input analog voltage. Such fluctuations are randomly distributed among the sub-ADCs (SADCs), and there is a positive or negative shift.

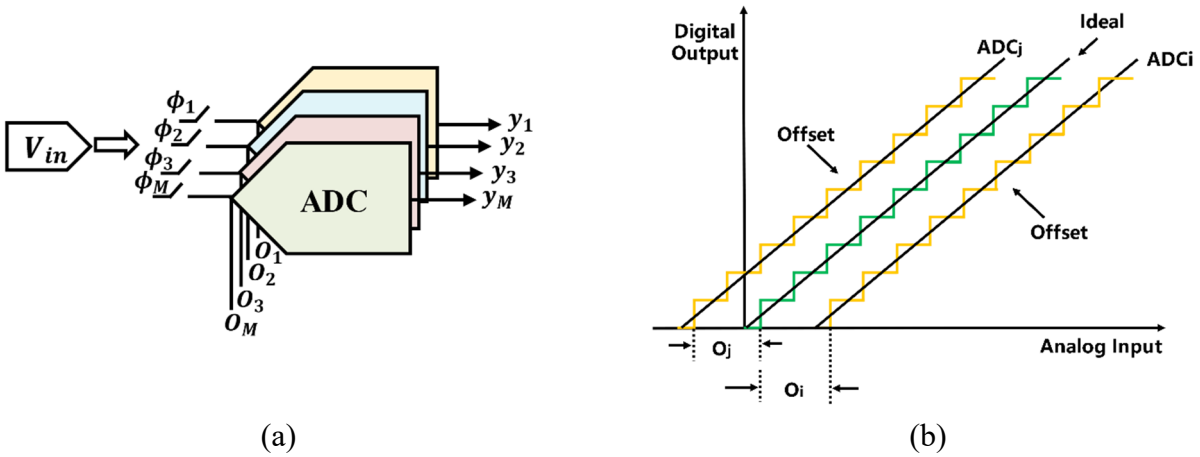


Figure 3. (a) Conversion model with offset mismatch; (b) Transfer curve under ideal and offset mismatch case.

Each channel has a different offset mismatch $O_1, O_2, \ldots, O_M$, since each channel works alternately, the offset mismatch can be seen as periodic noise, which can be expressed as:

$$\{\ldots, O_1, O_2, \ldots, O_M, O_1, O_2, \ldots, O_M, O_1, O_2, \ldots\} \tag{1}$$

in the time domain, the noise sequence can be expressed as:

$$y(t) = \sum_{i=1}^{M} O_i \sum_{n=-\infty}^{\infty} \delta(t - kT_s - nMT_s) \tag{2}$$

where T_S is the sampling period, in order to identify the influence of the harmonics caused by the offset mismatch, Fourier transform of Eq (1) can be represented as:

$$\tilde{O}_n = \frac{1}{M} \sum_{i=-\infty}^{M-1} O_i e^{-j(\frac{2\pi}{M})ni} \tag{3}$$

bring Eq (3) into the output signal:

$$Y(j\omega) = \frac{2\pi}{T_S} \sum_{n=-\infty}^{\infty} \tilde{O}_n \, \delta(\omega - \frac{2\pi n}{MT_S}) \tag{4}$$

it can be seen from Eq (4) that the offset mismatch will produce harmonic components at $i \times f_S/M$, $i = 0,1,2,\ldots,M-1$, f_S is the sampling frequency, since the DFT has symmetry, this article takes the spectrum of one side, and the harmonics of the other half are the same. When the ADC only has an offset mismatch, for example, simulate the offset in the 4-channel ADC, we set the root mean square (RMS) and the range of offset to 0.29 V and $\pm$ 0.5 V respectively, Figure 4(a),(b) show the comparison between ideal and mismatch sampling sequence, the offset mismatch of each channel is different, and they all deviate from the ideal sampling point. As shown in Figure 4(c),(d), the spectrum contained M-1 harmonic components.

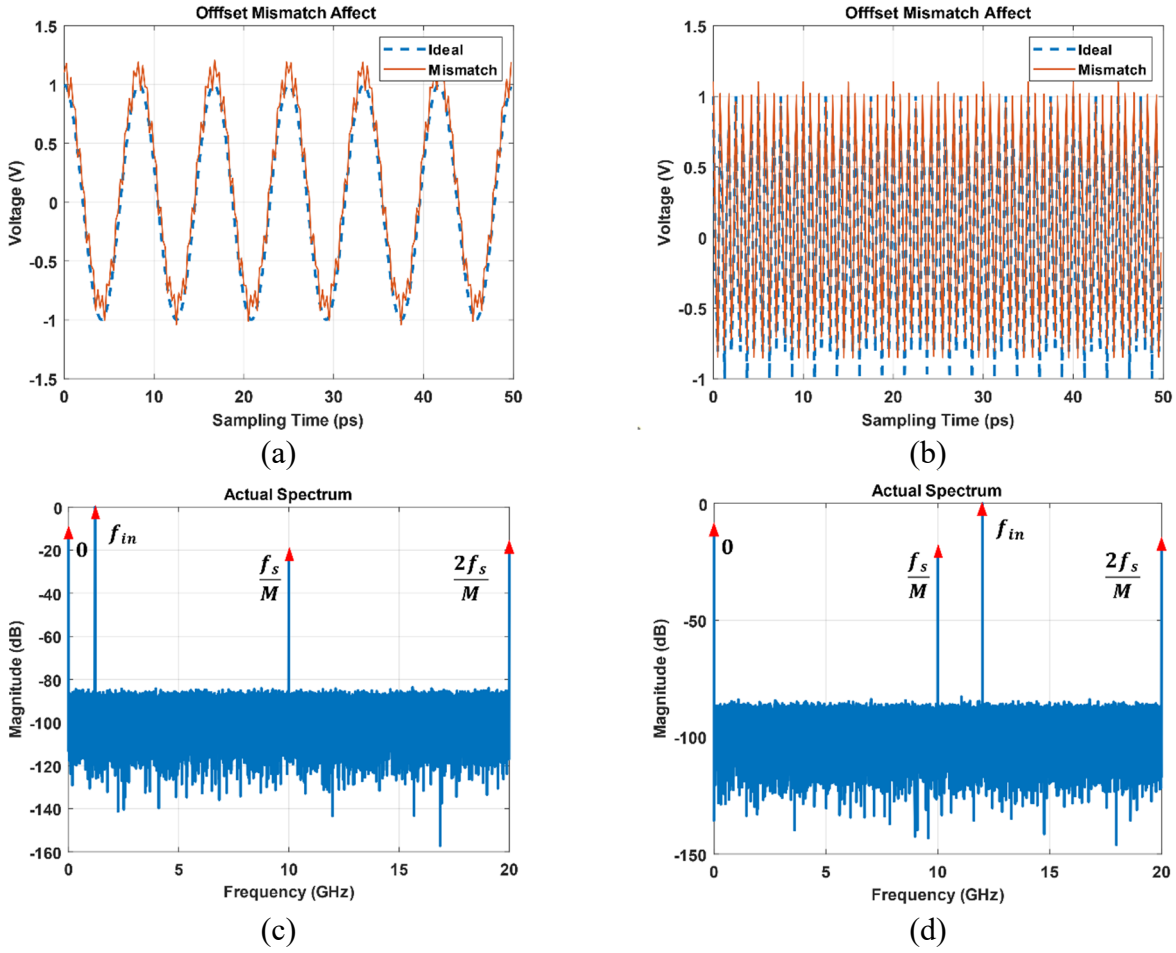
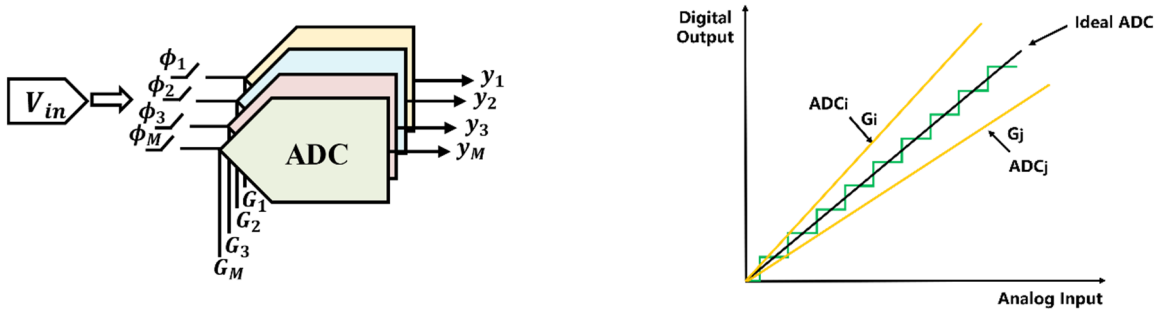


Figure 4. Sampling sequence with offset mismatch: a) f_{in} = 1.2 GHz, b) f_{in} = 12 GHz; Spectrum with offset mismatch: c) f_{in} = 1.2 GHz, d) f_{in} = 12 GHz.

2.2. Analysis of gain mismatch

The gain mismatch is generally caused by the mismatch of the ADC reference voltage, capacitance or device, the amplitude of the output signal is inconsistent with the ideal case, it is just a

ratio without unit. The ADC used in this article integrates 128 SADCs, each 8 SADCs are combined to form 16 channels. Due to the different positions of the SADCs on the chip, uneven temperature and unbalanced forces, each ADC has a randomly distributed gain mismatch. In an ideal case, the gain is 1, but due to the above reasons, the gain of each channel is randomly distributed within a certain range above or below 1. The mismatch model is shown in Figure 5(a), and Figure 5(b) shows a comparison between ideal transfer curve and actual curve with gain mismatch.



(a) (b)

Figure 5. (a) Conversion model with gain mismatch; (b) Transfer curve under ideal and gain mismatch case.

Each sub-channel ADC has a different gain $(G_1, G_2, \ldots, G_M)$. As shown in Figure 5(a), due to the periodic alternating work of each channel ADC, the gain mismatch can be seen as the sequence noise, which can be expressed as:

$$\{\ldots, G_1, G_2, \ldots, G_M, G_1, G_2, \ldots, G_M, G_1, G_2, \ldots\} \tag{5}$$

in time domain, Eq (5) is represented as:

$$a(t) = \sum_{i=0}^{M-1} G_i \sum_{n=-\infty}^{\infty} \delta(t - kT_S - nMT_S) \tag{6}$$

in order to facilitate analysis, Eq (6) is transformed into frequency domain after Fourier transform:

$$A_n = \frac{1}{M} \sum_{i=0}^{M-1} G_i e^{-j(\frac{2\pi}{M})ni} \tag{7}$$

assume there is only a gain mismatch in the time-interleaved ADC system, the output sequence can be expressed as:

$$Y(j\omega) = \frac{1}{T_S} \sum_{n=-\infty}^{\infty} A_n X[j(\omega - \frac{2\pi n}{MT_S}] \tag{8}$$

gain mismatch will cause the nonlinearity of the time-interleaved ADC output, which appears as periodic noise in the time domain, and as high-energy harmonics at a fixed frequency in the frequency domain. The frequency position where the peak of the harmonic spectrum appears for:

$$f_{dis} = \pm f_{in} + \frac{i}{M} f_S, i = 1,2, \ldots, M-1 \tag{9}$$

In the simulation with gain mismatch only, we set the RMS to 1.01, and the range of the gain mismatch is $\pm$ 1.30, the sampling sequence is shown in Figure 6(a),(b). The inconsistency of the gains between the 4 channels causes the sampling point to deviate from the ideal sampling point. The mismatched spectrum is shown in Figure 6(c),(d). Large harmonic components are produced at the frequency $\pm f_{in} + i \times f_s/M$, which have an impact on the signal, different input frequencies lead to different harmonic positions within a limited spectrum.

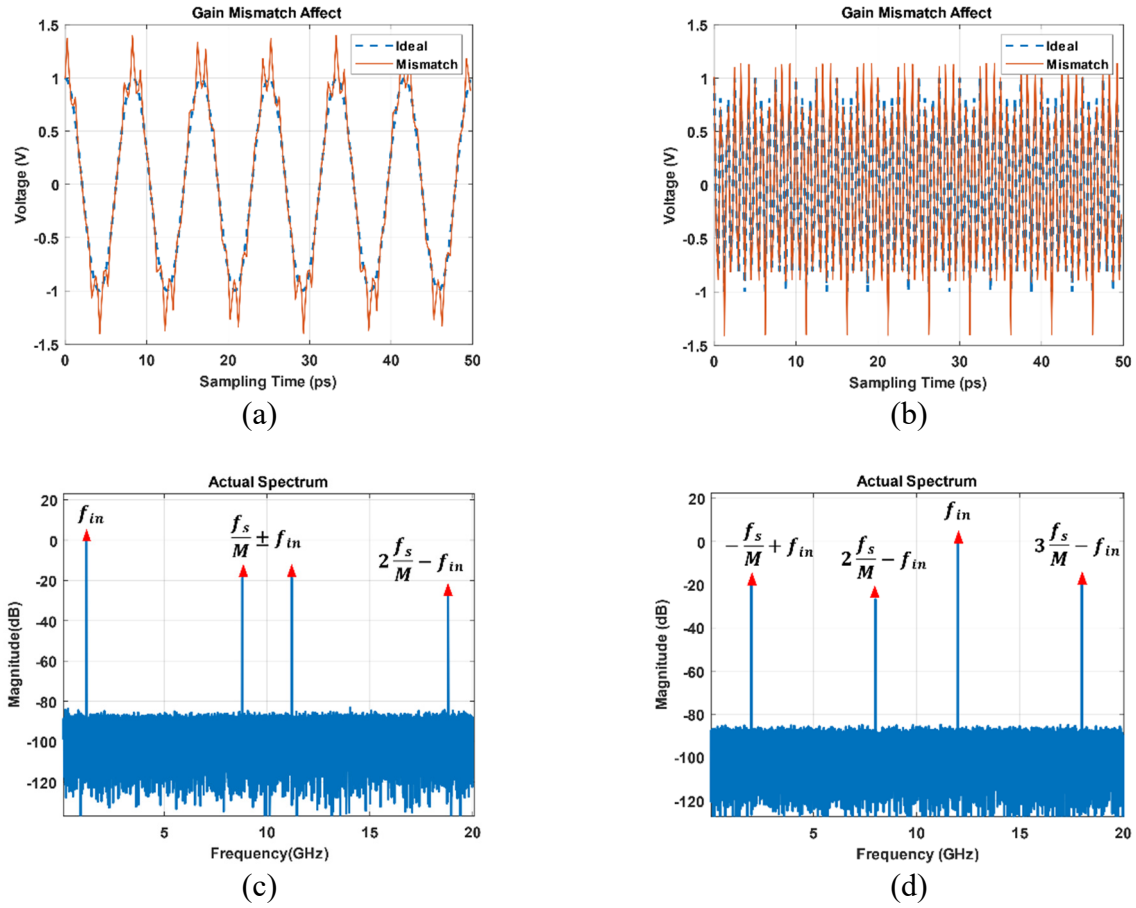


Figure 6. Sampling sequence with gain mismatch: (a) f_{in} = 1.2 GHz, (b) f_{in} = 12 GHz; Spectrum with gain mismatch: (c) f_{in}=1.2 GHz, (d) f_{in} = 12 GHz.

2.3. Analysis of clock jitter

The jitter of the clock causes delay in the sampling time of different channels, the clock diagram with time delay is shown in Figure 7(a), which make the actual sampling point deviate from the ideal sampling point shown in Figure 7(b).

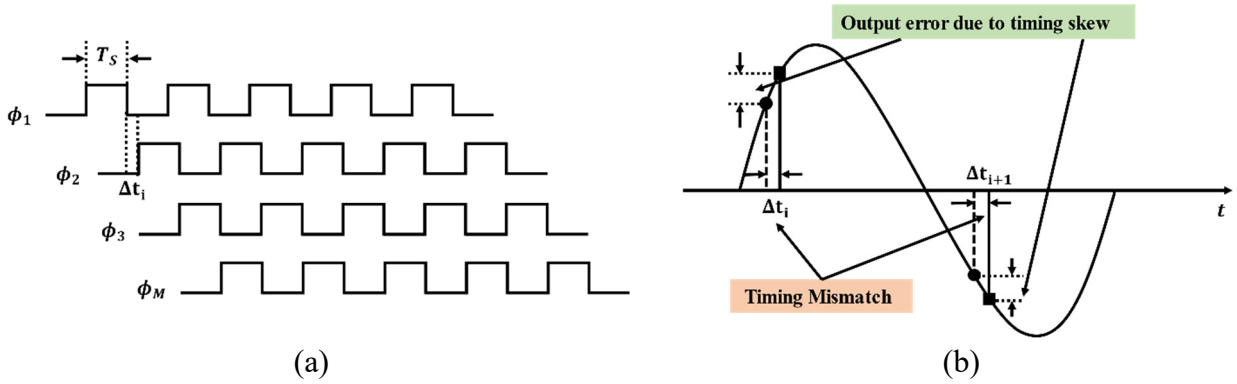


Figure 7. (a) Sampling clock diagram with clock jitter; (b) The clock jitter make sampling points deviate from ideal case.

The clock phase generated by the ideal clock is ϕ_i and the jitter is Δt_i, the sampling points are different from ideal case, the sequence can be expressed as:

$$y(t) = \sum_{i=0}^{M-1} y_i(t) = \sum_{i=0}^{M-1} \sum_{k=-\infty}^{+\infty} x(t - \Delta t_i)\delta(t - (nM + i)T_S), i = 0,1, \dots, M-1 \tag{10}$$

where $y_i(t)$ is the sampling sequence of channel i, $x(t)$ is the input signal, and $\delta(\cdot)$ is the sampling pulse sequence, $\delta(\cdot)$ can be represented in frequency domain as:

$$\sum_{k=-\infty}^{+\infty} \delta\left(j\left(\Omega - \frac{2\pi k}{MT_S}\right)\right) e^{-j\Omega i T_S} \tag{11}$$

As a result, $y(t)$ can be represented in frequency domain as:

$$\begin{aligned} Y(j\Omega) &= \frac{1}{T_S} \sum_{k=-\infty}^{+\infty} X(j(\Omega - \frac{k2\pi}{MT_S})) \sum_{i=0}^{M-1} \frac{1}{M} e^{\frac{-jki2\pi}{M}} e^{-j\Omega\Delta t_i} \\ &= \frac{1}{T_S} \sum_{k=-\infty}^{+\infty} \alpha[k] X(j(\Omega - \frac{k2\pi}{MT_S})) \end{aligned} \tag{12}$$

where $\alpha[k]$ can be represented as:

$$\alpha[k] = \sum_{i=0}^{M-1} \frac{1}{M} e^{-j\Omega\Delta t_i} e^{-\frac{jki2\pi}{M}} \tag{13}$$

As we can know from Eq (13), the jitter of sampling clock can cause several harmonic components at $\pm f_{in} \pm if_S/M$ $(i = 1,2,\ M-1)$ in the spectrum, in the simulation, we set the RMS to 14.53 ps, and the clock jitter range is $\pm 1/f_S$, as shown in Figure 8(a),(b), the sampling points are different from the ideal case, the position of harmonic components are consistent with the above derivation, which are shown in Figure 8(c),(d).

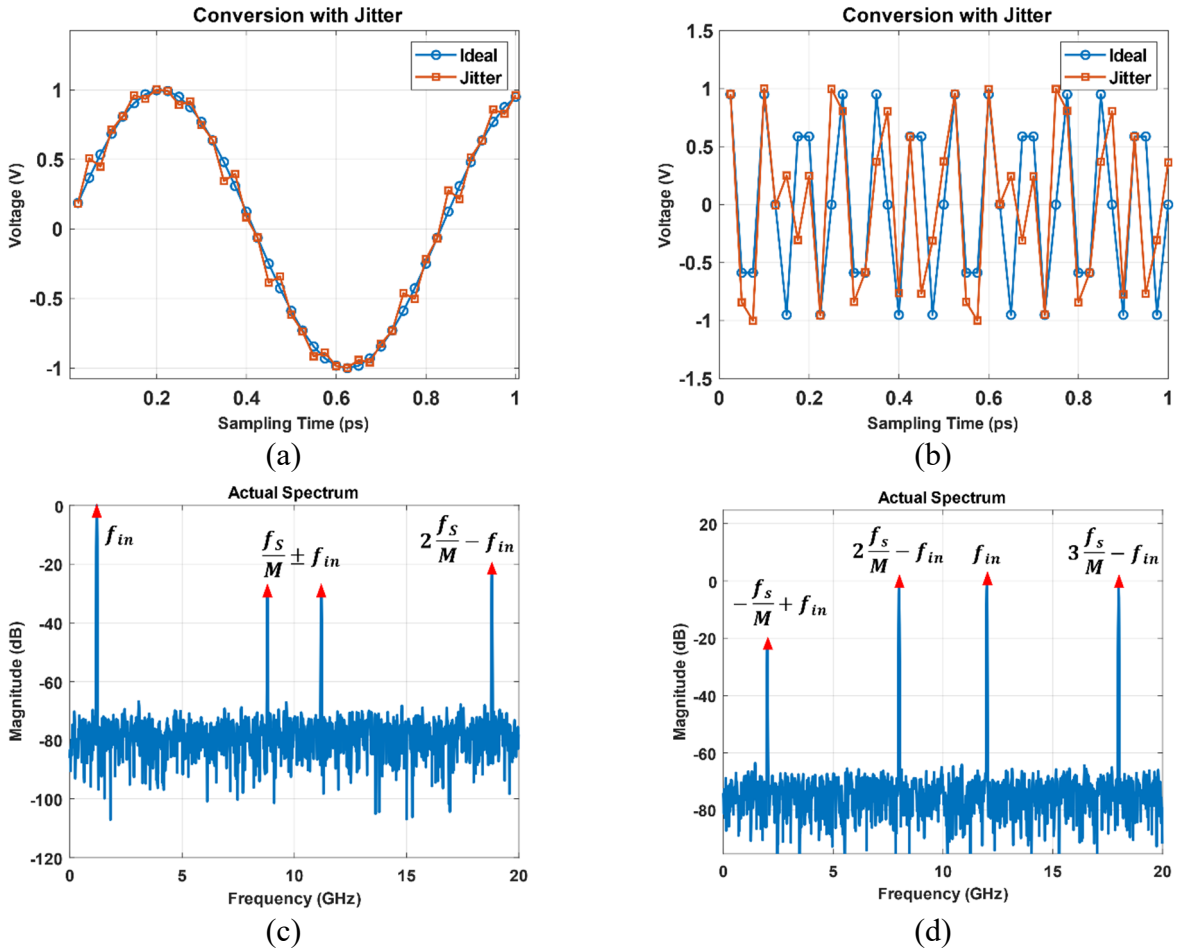


Figure 8. Sampling sequence with clock jitter: (a) f_{in}= 1.2 GHz, (b) f_{in} = 12 GHz; Spectrum with clock jitter: (c) f_{in} = 1.2 GHz, (d) f_{in} = 12 GHz.

The energy of the effective signal in the output spectrum can be represented as:

$$P_S = 2|\alpha[0]|^2 = 2\left|\frac{1}{M}\sum_{i=0}^{M-1} e^{j\Omega_0 \Delta t_i}\right|^2 \tag{14}$$

The noise power caused by clock jitter can be represented as:

$$P_N = 2\sum_{i=1}^{M-1}|\alpha[k]|^2 = 2\sum_{i=0}^{M-1}|\alpha[k]|^2 - 2|\alpha[0]|^2 \tag{15}$$

According to the Parseval theory,

$$2\sum_{i=1}^{M-1}|\alpha[k]|^2 = 2\frac{1}{M}\sum_{i=0}^{M-1}\left|e^{-j\Omega_0 \Delta t_i}\right|^2 = 2 \tag{16}$$

As a result, the SNR can be represented as:

$$SNR = 10\,log_{10}\left(\frac{P_S}{P_N}\right) = 10\,log_{10}\left(\frac{\beta_1^2 + \beta_2^2}{1 - \beta_1^2 - \beta_2^2}\right) \tag{17}$$

where $\beta_1 = \frac{1}{M}\sum_{i=0}^{M-1}\cos(\Omega_0 \Delta t_i)$, $\beta_2 = \frac{1}{M}\sum_{i=0}^{M-1} sin(\Omega_0 \Delta t_i)$, Eq (17) shows that noise and input

frequency can influence the SNR seriously.

3. Review of channel equalization algorithm

3.1. Offset mismatch calibration using equalization algorithm

According to the channel equalization method, we construct the offset mismatch calibration diagram shown in Figure 9. The model ACC&AVG indicates the accumulative average method. The specific process is:

- According to the accumulative average method, calculate the initial offset mismatch $O_i(i = 0,1,\dots,M-1)$ according to Eq (18), and obtain D_o by taking the difference between O_i and O_{ref},

$$O_i = \frac{N}{M} \cdot (s_i + \sum_{n=1}^{N/M} s_{nM-i}) - s_0, i = 0,1,\dots,M-1 \tag{18}$$

$$D_0 = O_i - O_{ref}, O_{ref} = 0\ V \tag{19}$$

- where s is the actual sampling sequence, M is the number of channels, N is the total number of sampling points, and s_0 is the direct current (DC) offset of the signal under ideal case, $O_{ref} = 0$.
- According to Eq (20), the offset correction amount $O_{cal,t}$ is initialized, the result is stored in the register, and $O_{cal,t}$ is updated according to Eq (21).

$$O_{cal,1} = \mu_g \times D_o \tag{20}$$

$$O_{cal,t} = \mu_o \times D_o + O_{cal,t-1} \tag{21}$$

where μ_o is the calibration step size, which determines the number of iterations and calibration accuracy of the calibration algorithm.

- Calibrate the output data according to $O_{cal,t}$ to get the updated sequence $y_{out,i}$.

$$y_{out,i} = s_{out,i} - O_{cal,t-1} \tag{22}$$

Update the calibrated data to D_o once in step 2 and repeat the above algorithm, until O_i approaches O_{ref} and O_{cal} approaches a fixed value.

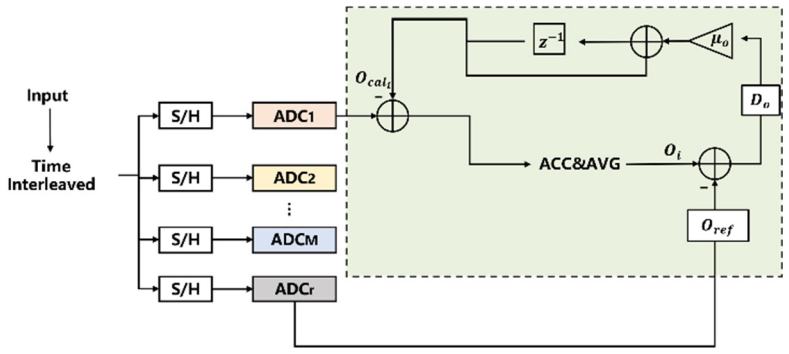


Figure 9. Traditional offset mismatch calibration method with accumulative average algorithm.

3.2. Gain mismatch calibration using equalization algorithm

Similar to the calibration of offset mismatch, the gain calibration is shown in Figure 10. The specific derivation process is presented as follows:

- According to the accumulative average, the gain mismatch G_i is initialized according to Eq (23), and the difference between G_i and G_{ref} is expressed by D_g:

$$G_i = \frac{M\sum_{n=1}^{\frac{N}{M}}(s_{nM-i}^2 + s_i^2)}{\sum_{i=0}^{M}\sum_{n=1}^{N/M}(s_{nM-i}^2 + s_i^2)} \tag{23}$$

$$D_g = G_i - G_{ref}, G_{ref} = 1 \tag{24}$$

- Initialize the gain correction amount G_{cal} according to Eq (25), and update G_{cal} according to Eq (26):

$$G_{cal} = \mu_g D_g \tag{25}$$

$$G_{cal,t} = \mu_g D_g + G_{cal,t-1} \tag{26}$$

where μ_g is the calibration step size, which determines the number of iterations and calibration accuracy of the calibration algorithm.

- Use G_{cal} to calibrate the signal to get the updated sequence $y_{out,i}$:

$$y_{out,t} = s_{out,i} \times (G_{cal,t} - 1) \tag{27}$$

- Update the calibrated data to D_g once in step 2 and repeat the above algorithm. G_i approaches G_{ref}, G_{cal} approaches a fixed value, and the calibration is completed.

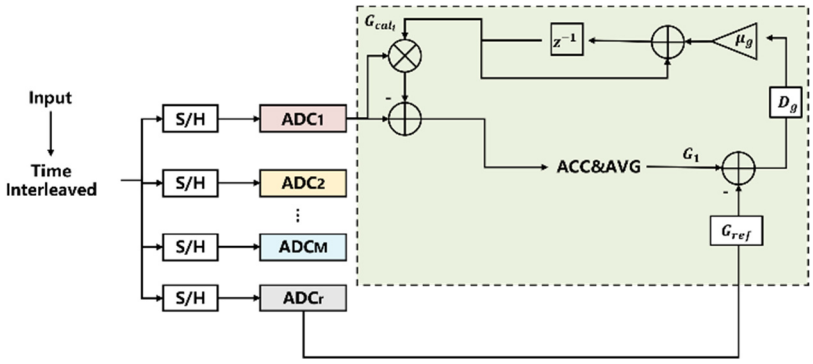


Figure 10. Traditional gain mismatch calibration method with accumulative average algorithm.

4. Mismatch estimation and calibration based on Monte Carlo method

Monte Carlo method, also known as statistical simulation method, is a general term for ideas or methods, rather than algorithms in the strict sense [28,29]. The advantage of this method is that it can better deal with the randomness problem in the communication system: the mismatch of each channel is stable and unchanging, and the constant characteristics can be used to iterate; but the quantized noise

is different in each measurement, and noise varies non-linearly with time, which is in line with the characteristics of probability and statistics. Follow the steps below to build a Monte Carlo model:

- Construct or describe the random process: The random noise generated by the mismatch allows the probabilistic process to be established, although each ADC has its own different true value of mismatch, but the result of each estimated mismatch is random.
- Sample from a known probability distribution: Because the estimated mismatch noise is different each time, the output result of ADC_i is different, but the sequence noise is periodically randomly distributed and has regularity.
- Obtain estimation results.

The estimation diagram is shown in Figure 11. The input signal $x(t)$ is sampled by ADC to obtain $y[n]$, and $y[n]$ is subjected to least square fitting. The gain mismatch g_i, offset mismatch os_i and time delay Δt_i are included in the parameters $\hat{A}, \hat{B}, \hat{C}$; the ideal sequence is interpolated by finite impulse response (FIR), after the mismatch model, the unknown mismatch $\Delta t_i, g_i, os_i$ are added and the actual output sequence is equal, and the equation is constructed and solved using the equal relationship between them.

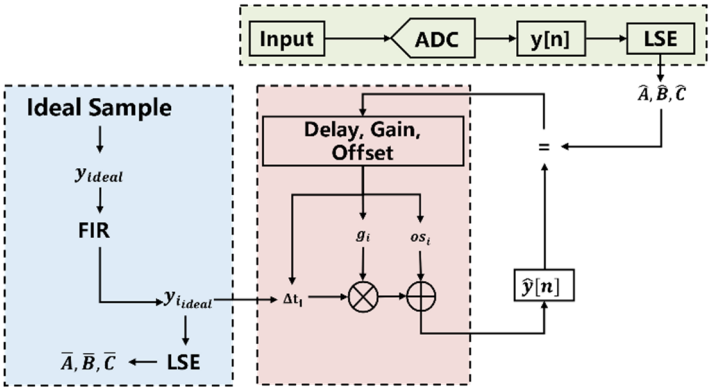


Figure 11. Channels' mismatch estimation diagram.

The specific solution process is as follows: the ideal input signal can be expressed as:

$$x(t) = acos(2\pi f_{in} t + \phi) + C \tag{28}$$

where α is the signal amplitude, f_{in} is the signal frequency, ϕ is the phase, and C is the DC bias. The actual sampling sequence can be expressed as:

$$y[n] = Q\left[\alpha\, cos(\omega n + \phi) + C + e[n]\right], n = 0, \ldots, N-1 \tag{29}$$

where Q is the quantization parameter, $Q = \frac{V_{FS}}{2^n}$, $\omega = \frac{2\pi f_{in}}{f_s}$, $e(n)$ is the channel noise, and N is the number of sampling points. The actual output of ADC_i is:

$$Y_i = \left[y(i), y(i + 1 * M), \ldots, y\left(i + \frac{N}{128} * M\right)\right] \tag{30}$$

There are many ways to estimate parameters. This article uses least square (LS) to complete fitting. By calculating the minimum value of Eq (31), the best estimation result is:

$$(E)^2 = \sum_{n=0}^{N-1} (y[n] - \hat{y}[n])^2 \tag{31}$$

where $y[n]$ is the actual sampling sequence, $\hat{y}[n] = \hat{\alpha}\cos(\omega n + \hat{\phi}) + \hat{C} = \hat{A}\cos(\omega n) + \hat{B}\sin(\omega n) + \hat{C}, \hat{A} = \hat{\alpha}\cos(\omega n), \hat{B} = \hat{\alpha}\, sin(\omega n)$. The actual output after fitting is:

$$y_i[n] = \hat{A}_i\, cos(\omega_i n) + \hat{B}_i\, sin(\omega_i n) + \hat{C}_i, n = i, i+m, \ldots, i + \frac{NM}{128} \tag{32}$$

For the case of no mismatch between ADC_s, the output of ADC_i can actually be understood as the output of ADC_0 obtained through n-fold interpolation [30,31]. Therefore, when performing LS fitting on an ideal channel, an ideal sequence can be obtained through an interpolation filter. This article uses Chebyshev I-type interpolation filtering to simulate two-channel ADC interpolation. First, ADC_1 is twice interpolated, and the upper limit of passband lost is set $R_p = 0.1$, the lower limit of stopband loss is $R_s = 1$, and the normalized band angle frequency $W_p = 0.4$, the stopband corner frequency $W_s = 0.6$, after calculated through the above parameters, the filter order $n = 2$ and the cutoff frequency $f_p = 0.4$, besides, as shown in Figure 12, the interpolated filter is compared to the initial sequence, the filter contains more points and the error would be reduced.

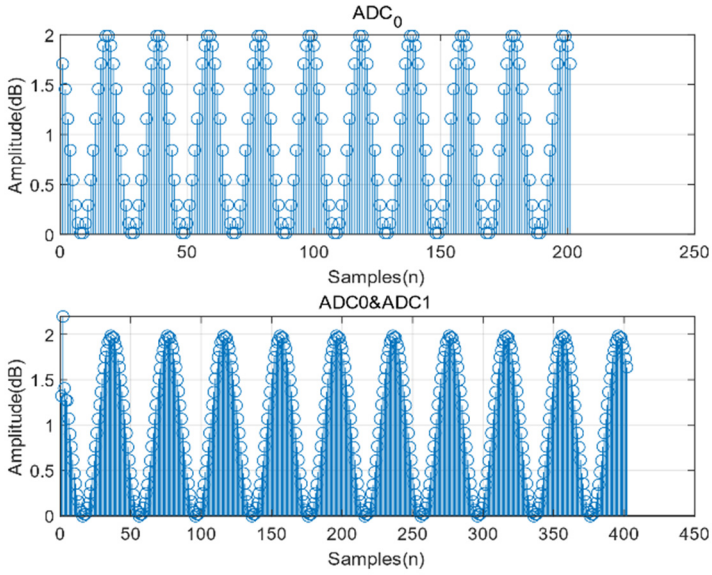


Figure 12. Sampling points before and after interpolation.

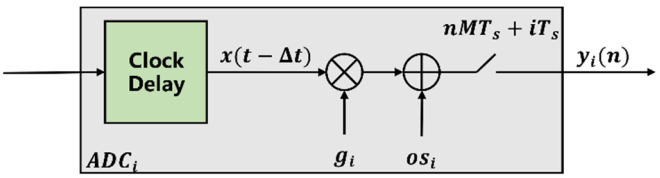


Figure 13. Sampling diagram in channels with different mismatch.

Fit the output data without mismatch according to the result of interpolation, and the fitted sequence of ideal ADC_i can be represented as:

$$\bar{y}_i[n] = \bar{A}_i\, cos(\omega_i n) + \bar{B}_i\, sin(\omega_i n) + \bar{C}_i, n = i, i+m, \dots, i+\frac{NM}{128} \tag{33}$$

where $\bar{A}_i = \bar{\alpha}_i \cos(\bar{\phi}_i)$, $\bar{B}_i = \bar{\alpha}_i \sin(\bar{\phi}_i)$.

In order to construct a set of equations, add mismatches to the ideal sequence according to Figure 13, add the delay Δt_i between ADCs, the offset mismatch os_i and the gain mismatch g_i one by one [11]. Due to the presence of noise and mismatch in the channel, the actual output sequence can be expressed as:

$$y_i[n] = g_i \cdot x(nMT_s + iT_s + \Delta t_i) + os_i, i = 0,1,2, \dots, M-1 \tag{34}$$

substituting the $x(t)$ expression into Eq (34), $y_i(n)$ can be expressed as:

$$\begin{aligned} y_i[n] &= P\, cos(\omega_0 n) - Q\, sin(\omega_0 n) + \bar{C}_i + os_i \\ P(\cdot) &= [\bar{A}_i g_i\, cos(2\pi f_{in}\Delta t_i) + \bar{B}_i g_i\, sin(2\pi f_{in}\Delta t_i)] \\ Q(\cdot) &= [\bar{A}_i g_i\, sin(2\pi f_{in}\Delta t_i) - \bar{B}_i g_i\, cos(2\pi f_{in}\Delta t_i)] \end{aligned} \tag{35}$$

Equations (35) and (32) both represent the actual output of ADC_i, so the relationship between the ideal sine and the fitted actual sequence is:

$$\left[\hat{A}_i\ \hat{B}_i\ \hat{C}_i\right]^T = [\bar{A}_i\ \bar{B}_i\ \bar{C}_i]^T \cdot \bar{E} \tag{36}$$

where $\hat{A}_i\ \hat{B}_i\ \hat{C}_i$ and $\bar{A}_i\ \bar{B}_i\ \bar{C}_i$ are all known, matrix $\bar{E}$ can be represented as:

$$\begin{bmatrix} g_i\, cos(2\pi f_{in}\Delta t_i) & -g_i sin(2\pi f_{in}\Delta t_i) & 0 \\ g_i sin(2\pi f_{in}\Delta t_i) & g_i\, cos(2\pi f_{in}\Delta t_i) & 0 \\ 0 & 0 & 1 + os_i/\bar{C}_i \end{bmatrix} \tag{37}$$

Solve the matrix equation and get the expressions of g_i, Δt_i and os_i:

$$\begin{cases} \Delta t_i = tan\left(\dfrac{\hat{A}_i\bar{B}_i - \bar{A}_i\hat{B}_i}{\hat{A}_i\bar{A}_i - \bar{B}_i\hat{B}_i}\right)/2\pi f_{in} \\ g_i = \dfrac{\hat{A}_i}{\bar{A}_i\, cos(2\pi f_{in}\Delta t_i) + \bar{B}_i sin(2\pi f_{in}\Delta t_i)} \\ os_i = \hat{C}_i - \bar{C}_i \end{cases} \tag{38}$$

4.1. Offset calibration with Monte Carlo method

Pack the above algorithm into the model named *Cali*, replace the ACC&AVG module in the algorithm presented in Section 3, the detailed process is shown in Figure 14:

- The input signal enters M SADCs through time interleaving sampling, and the sampled sequence enters the *Cali*.
- The offset O_i of channel i is obtained by least square fitting and Monte Carlo estimation.
- The initial value of the offset calibration amount $O_{cal,t} = \mu_o D_o$.
- Compensate the sampling sequence according to $O_{cal,t}$, $y_{out,i} = s_{out,i} - O_{cal,t}$.

- Perform fitting and mismatch estimation on the compensated sequence, then update the mismatch O_i through the estimated result $EST_i = [g_i, os_i, \Delta t_i]$, the EST_i is calculated by Eq (38).
- Update the offset mismatch calibration amount $O_{cal,t} = \mu_o D_o + O_{cal,t-1}$.
- Compensate the sampling sequence again, $y_{out,i} = s_{out,i} - O_{cal,t}$;
- Repeat the above steps until O_i, D_o approach 0, $O_{cal,t}$ approach a constant value.

The above-mentioned calibration steps are calibrated ADC_i to ADC_M.

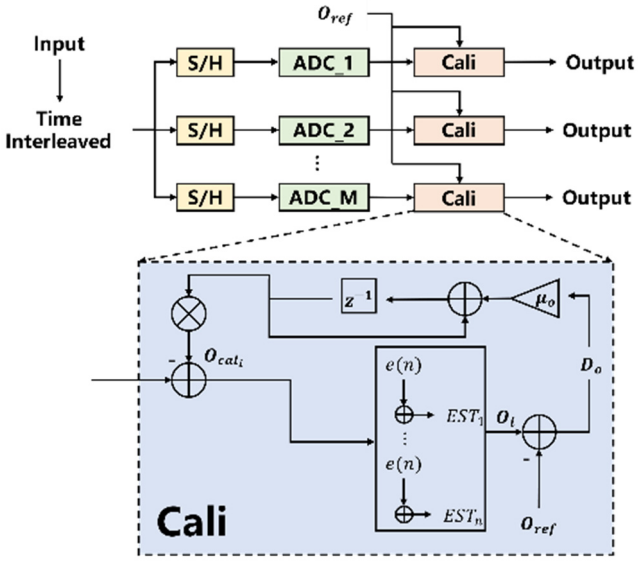


Figure 14. Offset mismatch calibration with Monte Carlo method.

4.2. Gain calibration with Monte Carlo method

Similar to calibrate the offset mismatch, calibrate the gain mismatch according to the diagram shown in Figure 15:

- The analog signal is input to M SADCs for interleaving sampling, and the sampling sequence output by ADC_i enters the model *Cali*.
- Fit the sequence and estimate the initial value G_i of the gain mismatch.
- The initial value of the gain calibration amount $G_{cal,t} = \mu_g D_g$;
- Compensate the sampling sequence according to $G_{cal,t}$, $y_{out,i} = s_{out,i} \times (G_{cal,t} - 1)$;
- Perform fitting and mismatch estimation on the compensated sequence, and update the gain mismatch G_i through the estimation result $EST_i = [g_i, os_i, \Delta t_i]$;
- Update gain mismatch calibration amount $G_{cal,t} = \mu_g D_g + G_{cal,t-1}$;
- Compensate the sampling sequence again, $y_{out,i} = s_{out,i} \times (G_{cal,t} - 1)$.

Repeat the above steps until G_i, D_g approach 0, and $G_{cal,t}$ approach a constant value. The above-mentioned calibration procedure is calibrated according to from ADC_i to ADC_M.

Compared with the inter-channel equalization algorithm proposed in Section 3, the reference channel set in this article is not a channel in the actual ADC, but an ideal ADC with offset mismatch $O_{ref} = 0\ V$ and gain mismatch $G_{ref} = 1$. In the calibrated process, all M channels are compensated, and the final sequence is close to the ideal value. The new reference channel does not occupy more logic resources and consume more power consumption; in addition, the initial mismatch will also be compensated in an iterative manner. Therefore, the accuracy requirements of this article are not as

strict as those mentioned in [7], and the accuracy of calibration mainly depends on the calibration factor μ. This method reduces the number of estimates and the amount of calculation.

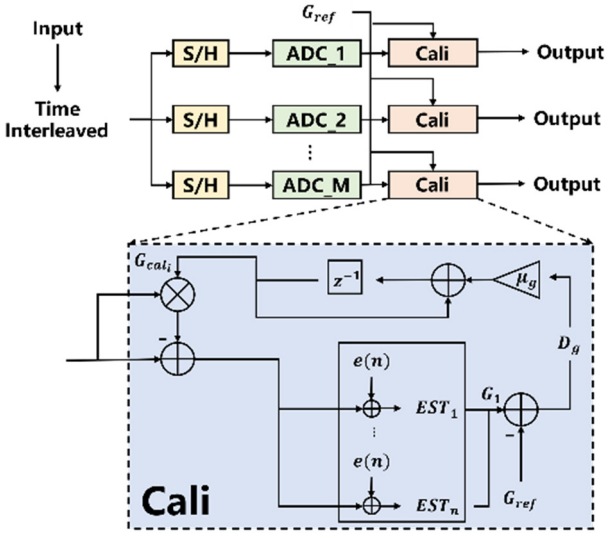
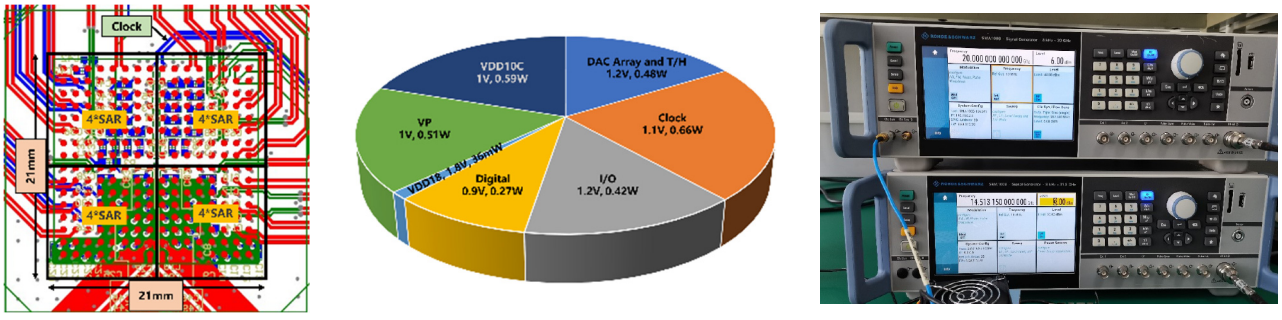


Figure 15. Gain mismatch calibration with Monte Carlo method.

5. Experiment results

The layout design and power consumption of the ADC are shown in Figure 16(a), and the size is 21 mm × 21 mm. The ADC is calibrated using the method in Section 4. The signal supply source is shown in Figure 16(b). The signal generator from Rohde Schwarz is used to input a 1.2 GHz and 5 dBm sinusoidal signal and enter the experimental platform through the RF interface. The actual platform is shown in Figure 16(c): The daughter card in the lower right corner is equipped with a 16-channel 8-bit ADC with a sampling frequency of 40 GS/s, and the reference voltage V_{ref} is 1.2 V, which is connected to the motherboard through the FPGA mezzanine card (FMC) interface, and the FMC connector establishes a connection with the FPGA through the gigabit transmitter in Y-version (GTY) high-speed port. The test environment and related indicators are shown in Tables 1 and 2:



(a) (b) (c)

Figure 16. (a) Chip Micrograph; (b) Power Breakdown; (c) The Signal Generator from Rohde Schwarz.

Table 1. Test environment.

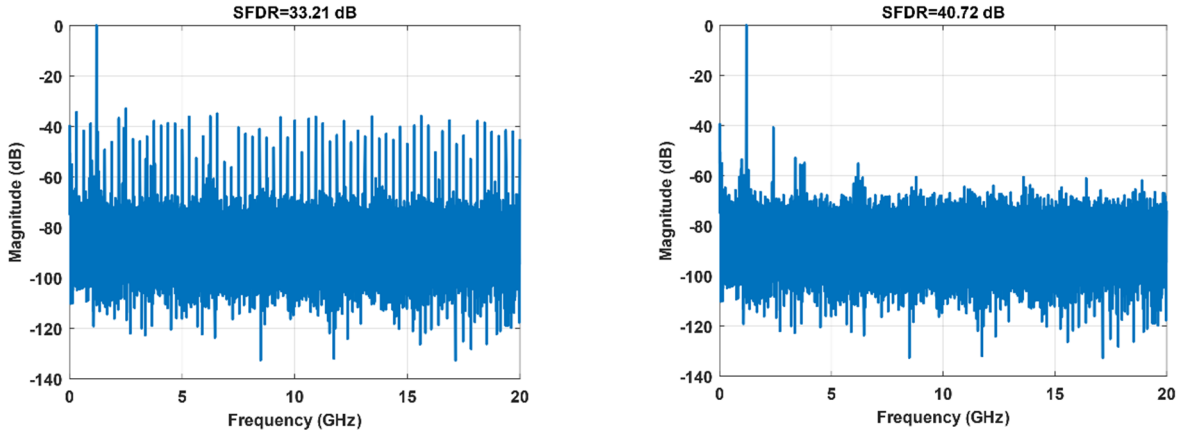
Hardware Configuration	Amount	Remark
Sampling Clock	1	$f_S > 15$ GHz
Input Signal	1	$f_{in} > 1$ GHz
High Frequency Cables	2	/
Balun	1	/
ADC Test Evaluation Board	1	40 GS/s 8-bit
FPGA	1	Xilinx Virtex
Computer	1	/

Table 2. Test target.

Parameter	Index
Resolution	8-bit
Sampling Frequency	40 GS/s
Number of Channels	16
Analog Input Bandwidth	1.2 GHz
SFDR	32 dB
ENOB	4.5 bits
Package	Flip Chip Ball Grid Array (FC BGA) 256
Size	21 mm × 21 mm × 2.53 mm
Pitch	1.27 mm
Output Interface	(Current Mode Logic) CML
Static Level	1C

5.1. Offset calibration

On the premise that the channel is aligned, the offset mismatch is calibrated. The spectrum before and after calibration is shown in Figure 17. The harmonic components are suppressed and the SFDR is improved. The other parameters are shown in Table 3.



(a) (b)

Figure 17. Spectrum before and after offset calibration.

Table 3. Performance of offset calibration.

Testing Parameters	Before Calibration	After Calibration	Units
SINAD	21.65	30.16	dB
SNR	21.91	30.58	dB
SFDR	34.51	40.72	dB
ENOB	4.21	5.76	bits

The experimental results show that the offset calibration algorithm is effective. The mismatch between channels is compensated.

After 100 iterations of the algorithm, the relationship between related parameters and the number of iterations is shown in Figure 18. Within the first 20 calibration iterations, the rate of change of the parameters is larger and the convergence speed is faster. After 50 iterations, it is basically stable. The offset mismatch O_i of each SADC approaches O_{ref}, and the difference D_o between the two approaches 0. The calibration value O_{cal} approaches a constant value, and the value is written into the M registers of the FPGA. The subsequent sampling sequence directly uses the register value, the result is compensated without iteration.

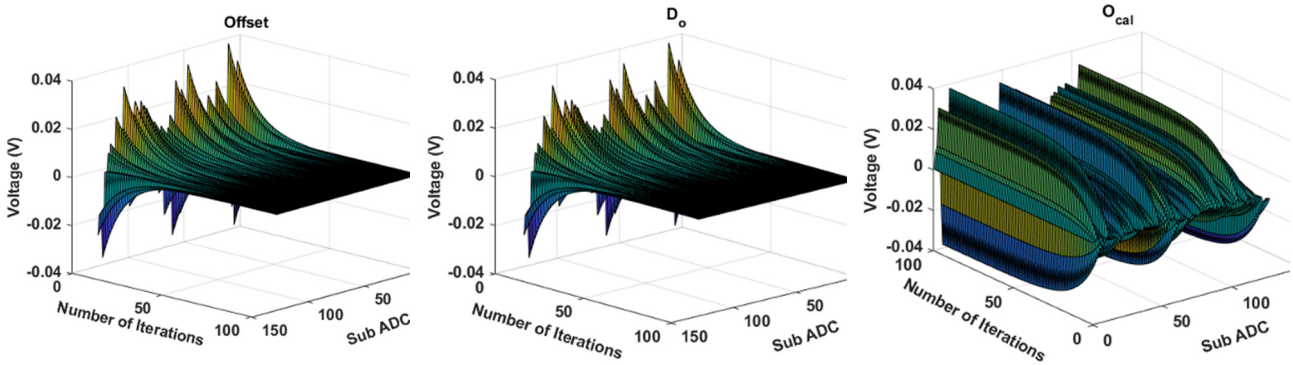
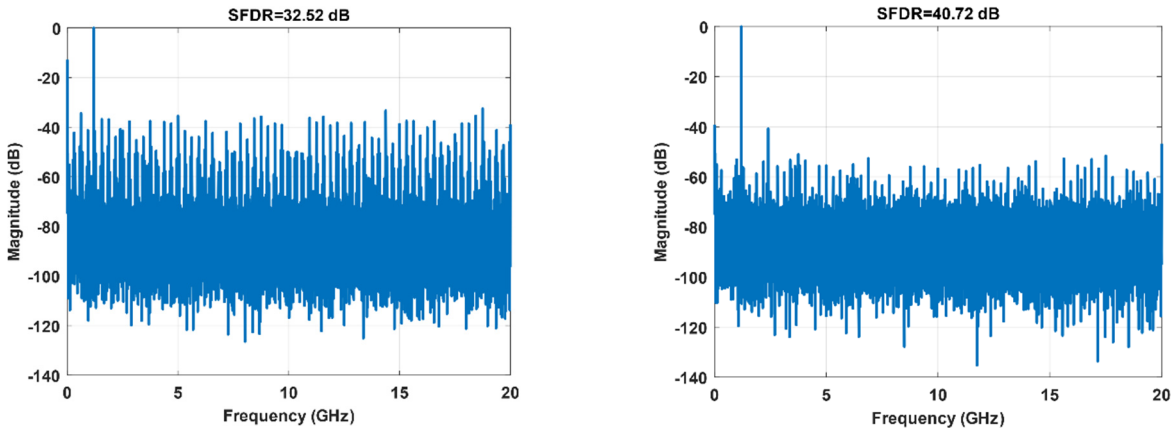


Figure 18. Parameters curve of different channels. (a) Offset mismatch O_i; (b) Offset error D_o; (c) Offset calibration amount O_{cal}.

5.2. Gain calibration

Compensate the sampling sequence according to the calibration algorithm of gain mismatch, and the spectrum is shown in Figure 19. The comparison before and after shows that the harmonic components are reduced after the algorithm. The test parameters are shown in Table 4. The experimental results show the algorithm in Section 4 is also effective in compensating for gain mismatch.



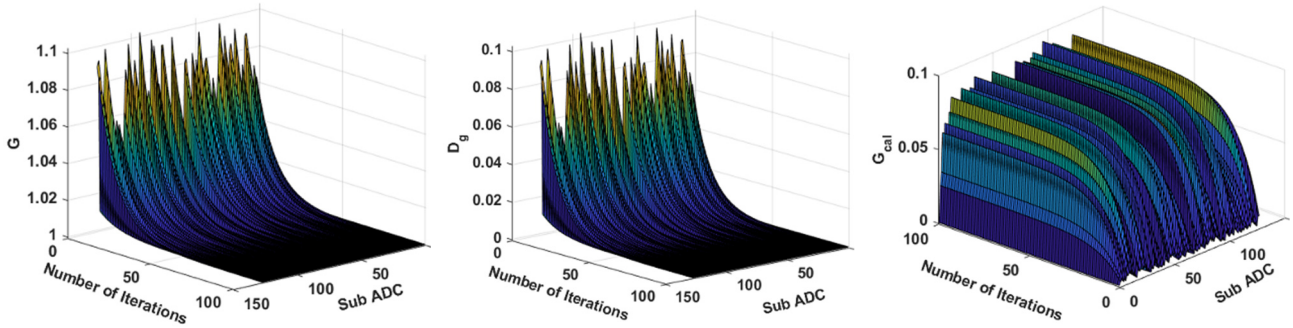
(a) (b)

Figure 19. Spectrum before and after gain calibration.

Table 4. Performance of gain calibration.

Testing Parameters	Before Calibration	After Calibration	Units
SINAD	21.00	29.68	dB
SNR	21.05	30.05	dB
SFDR	33.53	40.72	dB
ENOB	3.90	5.63	bits

Gain is the ratio of the output signal to the input signal without unit, so there is no unit of the relevant parameters. Similar to the offset calibration, after 100 iterations of the algorithm, the relationship between the relevant parameters and the number of iterations is shown in Figure 20, the calibration parameters within 20 times have a large change rate and a fast convergence speed. All parameters converge around 50 iterations, for each SADC, its gain mismatch G_i approaches G_{ref}, and the difference D_g approaches 0. The calibration amount G_{cal} approaches a constant value, and this value is written into the M registers of the FPGA. The subsequent sampling sequence directly uses G_{cal} to compensate the signal without calibration.



(a) (b) (c)

Figure 20. Parameters curve of different channels. (a) Gain mismatch G_i; (b) Gain error D_g; (c) Gain calibration amount G_{cal}.

The relationship curve between μ (μ_o and μ_g) and the number of iterations is shown in Figure 21. Although μ is less than 1, the number of iterations decreases with the increase of μ, which reduces the amount of calculation, but it affects the accuracy of calibration. When it is greater than 1, the number of iterations will increase accordingly. Therefore, setting μ appropriately can balance the calculation complexity and the calculation accuracy.

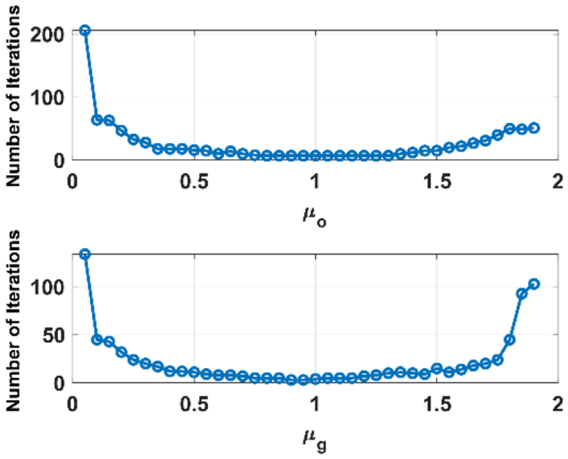


Figure 21. Variation curve of iteration times with μ_o and μ_g.

5.3. Comparison between this work and previous works

In order to verify the advantages proposed in this article, a series of comparative experiments are completed under the same conditions, the details are as follows.

The initial mismatch must be estimated before the calibration, the initial estimation accuracy affects the subsequent operations, we evaluate relative error after the first estimation, it is an average relative error of all SADCs, its unit is %, which can be represented as:

$$\delta = \frac{X_i - \bar{X}}{\bar{X}} \times 100\% \tag{39}$$

where δ is the relative error, X_i is the estimated mismatch, and $\bar{X}$ is the conventional true value of the mismatch after enough experiments. We compare the relative error with the accumulative average method and method proposed in 1241–2010 IEEE standard [26], in the standard, gain G and offset V_{OS} are represented as:

$$\begin{cases} G = \dfrac{Q(2^N-1)\left(\sum_{k=1}^{2^N-1} kT[k] - 2^{N-1}\sum_{k=1}^{2^N-1} T[k]\right)}{(2^N-1)\sum_{k=1}^{2^N-1} T^2[k] - \left(\sum_{k=1}^{2^N-1} T[k]\right)^2} \\ V_{OS} = T[1] + Q(2^{N-1}-1) - \dfrac{G}{2^N-1}\sum_{k=1}^{2^N-1} T[k] \end{cases} \tag{40}$$

where Q is the ideal width of a code bin, that is, the full-scale range divided by the total number of codes, N is the resolution of ADC, $T[k]$ is the input value corresponding to the transition between codes k and $k-1$. Table 5 shows the comparisons of relative errors, references [3] and [4] represent

the accumulative and average method, the Monte Carlo method in this article shows smaller relative error and higher estimation accuracy than others.

Table 5. Relative error of estimation compared with previous works.

Parameter (Gain/Offset)	This Work	[26]	[3]&[4]	Units
Relative Error	0.01/0.09	3.69/4.92	3.1/6.47	%

After estimating the initial mismatch, we also use the method presented in [3] and [4] to calibrate the ADC in the same experiment condition, the testing parameters are compared in Table 6, the proposed method has better calibration performance, higher accuracy and faster convergence than [3] and [4], the signal quality improves more and the harmonic components caused by the channel mismatch are suppressed.

Table 6. Performance comparison with previous works.

Parameters (Gain/Offset)	This Work	[3]&[4]	Units
SINAD	29.68/30.16	23.72/24.48	dB
SNR	30.05/30.58	23.81/24.59	dB
SFDR	40.7182/40.7187	37.56/37.46	dB
ENOB	5.63/5.76	5.08/4.75	bits
Number of Iterations	28/52	76/95	times

Furthermore, we verify the comparability of the two methods based on the measurement uncertainty u_A, which can be represented as:

$$u_A(x) = \sqrt{\frac{\sum_{i=1}^{n}(x_i - \bar{x})^2}{n(n-1)}} \tag{41}$$

where x is the measured quantity, $\bar{x}$ is the average of x, n is the number of measurements, the u_A of SINAD, SNR, SFDR and ENOB are listed in Table 7, which shows the possibility to compare this work with [3] and [4].

Table 7. Measurement uncertainty u_A.

u_A (Gain/Offset)	This Work	[3]&[4]	Units
SINAD	0.0064/0.0044	0.0067/0.0076	dB
SNR	0.0077/0.0053	0.0080/0.0088	dB
SFDR	0.0530/0.0455	0.0530/0.0532	dB
ENOB	2.03×10^{-4}/1.48×10^{-4}	2.14×10^{-4}/2.44×10^{-4}	bits

Some art works only present the method to calibrate gain mismatch, so we compare the gain error with other art works, different from the relative error, the gain error e_g is calculated after calibration and it is an absolute error, which can be represented as:

$$e_g = \frac{\sum_{i=1}^{M}(G_i - G_{ref})}{M} \tag{42}$$

where G_i is the gain of $SADC_i$ after calibration, M is the number of channels, this error represents the degree to which the calibrated signal is close to the ideal signal, which is also one of the indicators for judging the performance of calibration. As shown in Table 8, the gain error is smaller than previous works, shows better signal quality after calibration.

Table 8. Gain error comparison with previous works.

	This Work	[7]	[32]	[6]	[33]	[34]
e_g	0.0018	0.01	0.04	−0.015	−0.02	0.05

6. Conclusions

This article proposes a method that uses Monte Carlo to estimate the mismatch between ADC channels and combines the channel equalization method to calibrate the offset and gain mismatch. Such method does not need an actual channel as the reference, it is a global calibration, and there are no additional circuits. Compared with the accumulative average method, Monte Carlo method is more stable in the face of random noise. It can flexibly grasp the dynamic changes of transmitted data and does not require additional front-end processing circuits; besides, the estimation is more accurate compared to just average the mismatch, and high-precision estimation shortens convergence time. At a sampling frequency of 40 GS/s, a 16-channel TI ADC reaches an SFDR of 41 dB and an SNR of 30 dB, increases the ENOB from 4.06 bits to 5.68 bits, the performance is better than previous works (including IEEE Standard) at the same experiment condition. The results verify the novelty of the method, and highlight the advantages compared to other works in the literature, based on the high accuracy of estimation, this work increases the convergence speed, and saves more power consumption for the subsequent operations, such as frame synchronization, modulation format recognition and carrier recovery. As a result, it is an effective method in ADC calibration.

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Conflict of interest

We declare that we have no financial and personal relationships with other people or organizations that can inappropriately influence our work, there is no professional or other personal interest of any nature or kind in any product, service and/or company that could be construed as influencing the position presented in, or the review of, the manuscript entitled.

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