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Research article

Phase noise optimization of integrated ring voltage-controlled oscillators by metaheuristics

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Abstract: Real applications of integrated circuits (ICs) require satisfying strong target specifications, which challenge is focused on trading off specifications that are in conflict, i.e. improving one characteristic can degrade other(s). This is the case of designing a ring voltage-controlled oscillator (VCO) using IC nanometer technology, with the goal to accomplish a wide frequency and voltage-control tuning range, low silicon area, among others. For real ring VCO applications, an open challenge is guaranteeing minimum phase noise, which is in conflict with main dynamical characteristics when maximizing frequency range, voltage-control range, gain, and minimizing silicon area and power consumption. To cope with these design problems, we show the minimization of the phase noise of a ring VCO applying two metaheuristics, namely: Differential evolution (DE) and particle swarm optimization (PSO), which have the ability to handle constraints that are relevant to generate optimal solutions. The results show that both DE and PSO are effective in the optimization of the ring VCO. The comparison of the best phase noise results obtained with DE (-129.01 dBc/Hz @1MHz) and PSO (-124.67 dBc/Hz @1MHz) algorithms, not only show that the DE solution being lower by 4.34 dBc/Hz with respect to the best solution provided by PSO, but also it is quite satisfactory in contrast to similar works. Finally, the optimized ring VCO characteristics are compared herein with several designs considering a figure of merit, gain, frequency and voltage-control ranges.

Keywords: ring VCO; optimization; phase noise; differential evolution; particle swarm optimization
Mathematics Subject Classification: 26A33, 90C29

1. Introduction

Complementary metal-oxide-semiconductor (CMOS) technology is very suitable for real applications, as for example in the design of CMOS image sensors [1]. This type of integrated circuit

(IC) design involves analog and digital electronics, which static and dynamical characteristics can be accomplished by applying optimization techniques because a huge number of characteristics are in conflict. The CMOS design of analog ICs requires guaranteeing a proper static characteristic, which has been accomplished by applying optimization algorithms, as shown in [2]. This is not a trivial task in designing oscillators, as for the case of ring voltage-controlled oscillators (VCOs) that can be affected by process and temperature variations [3]. A VCO must work in a desired frequency range that is controlled by a voltage range, but it is dynamic so that one must find appropriate conditions to guarantee a robust design, e.g. guaranteeing minimum phase noise. Fortunately, metaheuristics are a good option to deal with problems whose target specifications are in conflict [4]. Another issue is considering constraints to reduce execution time of an optimization algorithm and improve convergence to the optimal solutions. In this manner, differential evolution (DE) and particle swarm optimization (PSO) algorithms have shown advantages in mono-objective optimization. For instance, the authors in [5] have shown that an objective condition may impose constraints on a design region, which make it difficult to find the exact optimal design, which can be solved by applying a multi-stage DE algorithm. In a similar direction, the authors in [6] introduced an improvement of PSO using artificial intelligence schemes. Both DE and PSO can also be combined as shown in [7].

VCOs find applications in a wide variety of integrated systems, so that they are very important blocks and henceforth its adequate design can greatly affect the performance of an application. From the IC design point of view, designing a ring VCO requires to take into account a variety of features that impact its electrical performance to different extents in accordance to a specific application that may require a wide frequency or voltage-control range. As mentioned above, process and temperature variations affect the dynamical behavior of a VCO, as well as other nonlinearities and second order effects that give place to identify trade-offs among IC design objectives [8, 9]. Therefore, both the trade-offs to be considered and the desired target specifications to be accomplished are important issues to achieve an optimal performance of a desired application.

In this paper we highlight that a low phase noise performance is the main desired feature in the robust design of a ring VCO. In the state of the art one can find that phase noise reduction is a strong challenge for ring VCOs, and it has been approached through various techniques [10–14]. However, depending on the application, in some cases the most relevant features can be related to achieving high frequency operation, wide frequency and voltage-control tuning range, low power consumption, minimal silicon area, VCO gain linearity, or robustness to process, voltage and temperature (PVT) variations [15]. Enhanced performances for a desired application can be achieved by using certain circuit topologies. This paper is orienting the effort to minimize phase noise of a ring VCO [16]. On this direction, some previous works have achieved phase noise reduction by adding passive elements, such as inductors or resistors, to a basic VCO topology, as shown in [8, 17, 18]. However, this may come at the cost of tuning range reduction, increased power consumption or greater silicon area. Other techniques regarding phase noise reduction in VCOs are sub-sampling loops [11, 19] that are applied in phase locked loops (PLLs). Superharmonic injection and current reuse [20, 21], are also used for this purpose aiming also for power reduction, however these can also result in a reduced tuning frequency range. As one can infer, minimizing phase noise involves important dynamical characteristics in optimizing a ring VCO, so that this is not a trivial task.

Through using optimization algorithms an IC designer can asses both the specifications and objectives simultaneously. Nowadays, algorithms such as machine learning have been used for

minimizing phase noise in a VCO considering PVT variations [22]. Other, previous and related works have employed metaheuristics to achieve phase noise minimization, some of them have combined optimization algorithms in conjunction with symbolic modeling, such as PSO, non-dominated sorting genetic algorithm (NSGAII), multi-objective particle swam optimization (MOPSO) and infeasibility-driven evolutionary algorithm (IDEA), to minimize both the phase noise and power consumption [23, 24]. Given that mono-objective algorithms are suitable for continuous optimization problems, such as the sizing of CMOS ICs [25, 26], and that the only objective for this case study is phase noise, mono-objective algorithms are selected to carry out the optimization. This is also due to the fact that since they use all of its capacity in the enhancement of a particular objective instead of purposing its power for the improvement of multiple objectives they can provide better results for the one objective [27]. Henceforth, two mono-objective algorithms, DE and PSO, are used herein with the objective to minimize phase noise in a ring VCO [28], which also accounts for trade offs, thus maintaining important features, such as minimum power consumption. It is important to mention that the use of metaheuristics for VCO optimization, such as DE and PSO, aims to offer the designer the possibility to redefine the algorithm's objective and constraints to the ones that are relevant to a particular application, without having to implement further design changes.

The paper organization is described next: Section 2 outlines the basis of DE and PSO algorithms. A brief description of the CMOS ring VCO to be optimized is presented in Section 3. The optimization algorithms adapted to minimize phase noise in a ring VCO are described in Section 4. Section 5 summarizes the optimization results. At last, the conclusions are presented in Section 6.

2. DE and PSO algorithms

2.1. Differential evolution

Differential evolution (DE) algorithm is based on the concept of individuals population's evolution through competition, by applying this conception an iterative optimization is carried out. The initial population is constituted by randomly generated individuals, each one of them represents a tentative solution. The individuals suitability for a particular problem is given by a fitness value, the relation between the individual and its fitness value is given by an objective function. New offsprings are generated by reproducing the individuals with better fitness (parents) by employing genetic operators, such as crossover and mutation which lead the algorithm towards finding suitable solutions. The survival of the offsprings is determined upon evaluation. The aforementioned process constitute a generation, and it keeps evolving until a stop criteria is met [4, 29].

Individuals are represented through vectors of real numbers, which are maintained within the defined limits of each design variable. If a design variable's value is not within the limits scope, the recombination and mutation operators can be used to reset the value. The algorithm's performance can be tuned to a faster convergence through its constants calibration. Through the optimization process each individual is mutated to generate an adaptive solution v_{ij} from three randomly chosen parents, as shown in (2.1). Subsequently, the crossover produces a trial solution through the recombination of a mutated solution v_{ij} with an individual x_{ij}, as done in (2.2). Last but not least, the replacement takes place by an elitist selection, which means that if the new individual's fitness value is better or equal to the parent, then the later will be replaced, as shown in (2.3) [4].

$$v_{ij} = x_{r3j} + P_f(x_{r1j} - x_{r2j}), \tag{2.1}$$

$$u_{ij} = \begin{cases} v_{ij} & \text{if} \quad rand_j[0,1] < P_c \quad \text{or} \quad j = j_{rand}, \\ x_{ij} & \text{otherwise}, \end{cases} \tag{2.2}$$

$$x_i(t+1) = \begin{cases} u_i(t+1) & \text{if} \quad f(u_i(t+1)) \leq f(x_i(t)), \\ x_i(t) & \text{otherwise}. \end{cases} \tag{2.3}$$

2.2. Particle swarm optimization

PSO is a mono-objective metaheuristic, that has been widely used for CMOS IC design. PSO initialization is performed from a particle disposition randomly generated within a defined search space, each particle is defined by its velocity and position [30]. The particles' velocity and position are represented by mathematical expressions. Regarding the particles' position, it varies through iterations from an initial velocity vector. Given that each particle recognizes its best position and determines if its actual position is the global best or if it is not, the particle's updating is based on both the particles' position and speed [25]. The particle's updating expressions are given by (2.4) and (2.5), where $p_i(t+1)$ and $v_i(t+1)$ are the particle's position and velocity at the i_{th} iteration, respectively. p_{best_i} and g_{best} represent the particle's best position and best global position, respectively. c_1 and c_2 depict the reliability of the particle in itself and in the swarm, respectively. Lastly, r_1 and r_2 are both real randomly generated numbers with a uniform distribution ranging within 0 and 1.

$$v_i(t+1) = v_i(t) + c_1 r_1(p_{best_i}(t) - p_i(t)) + c_2 r_2(g_{best}(t) - p_i(t)). \tag{2.4}$$

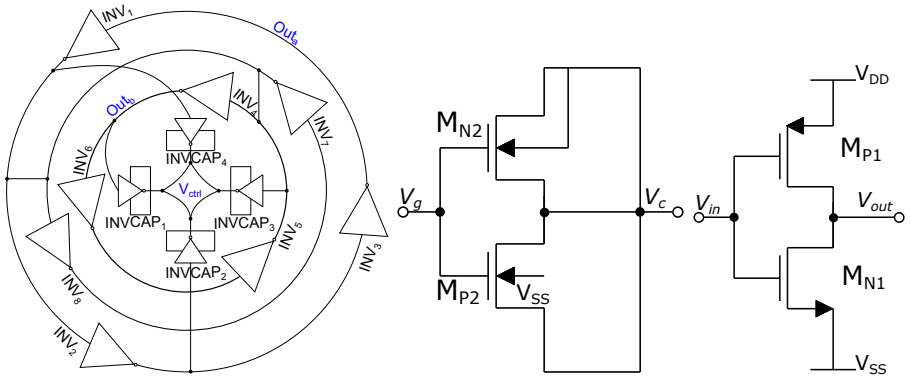
$$p_i(t+1) = p_i(t) + v_i(t+1). \tag{2.5}$$

The balance between exploration and exploration tendencies is given by constants c_1 and c_2. A rise in c_1 produces the particles to go towards its best local experiences, whereas an increase in c_2 results in faster convergence to the global best position [30]. Two factors that highly influence the achievement of global optimality are the selection of the best solutions that guarantees that an optimal value is reached, the other one is randomization, which prevents the solution from being stopped at optimum local values [31].

3. CMOS ring VCO

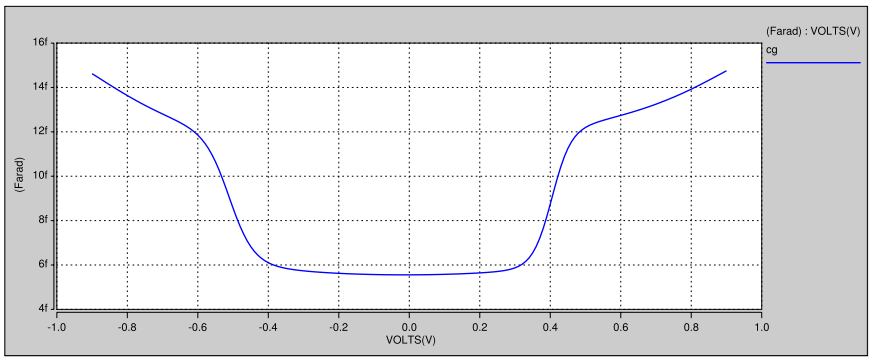
The case study of this paper is the phase noise minimization of the CMOS ring VCO topology shown in Figure 1(a) [32], this CMOS VCO is designed herein with a pseudo differential architecture using an IC technology of 180 nanometers (nm) from United Microelectronics Corporation (UMC). The VCO is implemented using the inverters shown in Figure 1(c) as delay cells, it is also composed by inverter caps, shown in Figure 1(b). Inverter caps are used to tune the VCO's oscillation frequency by varying the variable capacitance of the inverter's gate. Inverter caps benefit from having a desirable jitter performance, this is because they keep a fixed capacitance value through PVT variations [32].

Figure 2(a) shows the capacitance offered by the inverter cap circuit through the V_{gate} variation, the VCO tuning characteristics are shown in Figure 2(b).

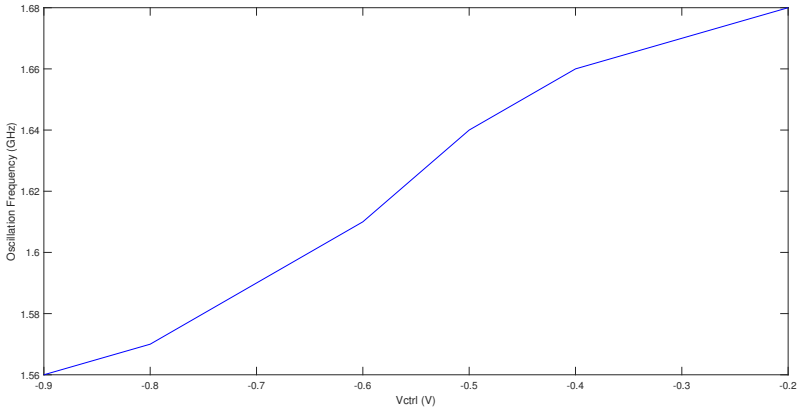


(a) (b) (c)

Figure 1. Eight stage ring VCO: (a) Schematic, (b) Inverter cap, and (c) Inverter.



(a)



(b)

Figure 2. Eight stages ring VCO: (a) Capacitance vs V_g, and (b) Tuning characteristics.

Before optimization of the VCO, it features -93.1 dBc/Hz @1MHz phase noise to begin with, an

oscillating frequency centered at 1.66 GHz with a 0.3 V control voltage, as shown in Figure 3.

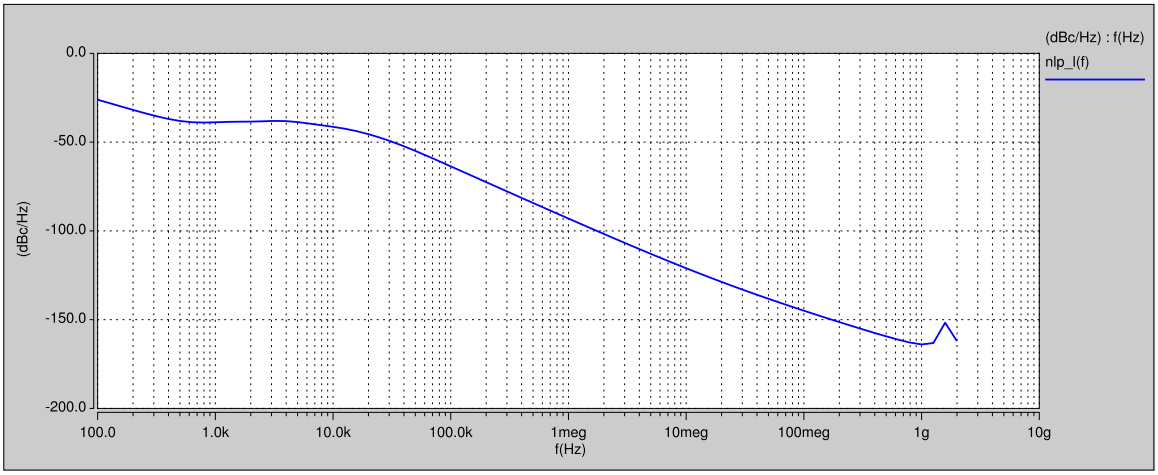


Figure 3. Phase noise of the eight stages VCO before optimization.

The transistors' sizes of the CMOS ring VCO preliminary design using an IC technology of 180 nm from UMC are: The inverter transistors have a gate channel width of $W_{MN1} = 9.45\ \mu m$, $W_{MP1} = 23.4\ \mu m$, and a gate channel length of $L_{MN1} = L_{MP1} = 0.27\ \mu m$. The inverter cap transistors sizes were set to $W_{MN2} = W_{MP2} = L_{MN2} = L_{MP2} = 2.7\ \mu m$. Thus resulting in oscillation frequencies between 1.68 GHz and 1.56 GHz, for voltages-control ranges between $-0.2\ V$ and $-0.9V$, respectively. The power consumption for this oscillator is around 11.34 mW at its highest frequency.

4. Optimization process description

In [9], the authors discussed a bi-objective problem considering that for an LC-VCO there is a trade-off between phase noise and power consumption, and both are minimized. Recent works show that DE [33] and PSO [34], can be improved. In this paper, the phase noise of the CMOS ring VCO shown in Figure 1(a) is minimized by applying DE and PSO algorithms. In this optimization problem, defined by (4.2), the single objective function is formulated as the phase noise minimization. Whereas the design variables, x, are constituted by the dimensions of both the inverter (W_{MP1}, W_{MN1}, L_{MN1}, L_{MP1}) and the inverter cap (in which case $W_{M2} = W_{MN2} = W_{MP2} = L_{MN2} = L_{MP2}$), as well as the voltage control range. The constraints are given by the operation region of the inverter MOS transistors [2], by the minimum frequency and maximum power consumption. The sizing optimization problem finds the most suitable sizes of the design variables that are within the defined search ranges, considering the restrictions' compliance.

$$g(x) = f(x) + \mu \sum r^2(x). \tag{4.1}$$

$$
\begin{aligned}
&\text{Search} : x = [W_{MP1}, W_{MN1}, L_{MN1}, L_{MP1}, W_{M2}, V_{ctrl}],\\
&Minimize : g(x),\\
&\text{Subject to} : f_{osc} > f_{min},\\
&P_{cons} < P_{max},\\
&V_{DS} \geq V_{GS} - V_{TH} \quad \text{for} \quad M_{N1} \quad \text{and} \quad M_{P1},\\
&W_{min} < W < W_{max},\\
&L_{min} < L < L_{max},\\
&V_{SS} < V_{ctrl} < V_{DD}.
\end{aligned}
\tag{4.2}
$$

For DE algorithm the objective function $g(x)$ in (4.2) is given by (4.1), where μ is a tunable constant that in this case is set to one, $r(x)$ represents the constraints and lastly $f(x)$ equals phase noise. Moreover, in the DE objective function, a flag sets a value of 0 or 1 for fulfilled and non fulfilled constraints, respectively, this means that when all of the restrictions are met the objective function is only determined by phase noise $g(x) = f(x)$. For the PSO algorithm the objective function is solely defined by the phase noise, meaning that for PSO $g(x) = f(x)$.

In both DE and PSO algorithms optimization processes, the phase noise measurement is carried out afterwards of the VCO simulation, where the operation region of the MOS transistors [2], the power consumption, and the oscillation frequency, are obtained. This is important, since the magnitude of the latter is required to measure phase noise through the HSPICE^{TM} RF command ".phasenoise". On the other hand, when the restrictions are not satisfied in the first run (e.g. VCO's oscillation frequency is lower than f_{min}, power consumption is greater than P_{max} or if the inverter MOS transistors are not working in the appropriate operation region) a high value is assigned to the VCO automatically. In this work, both algorithms DE and PSO provide good results by establishing this high value as phase noise=10^9, and it is assigned in both cases: When the constraints are not met and/or when the phase noise simulation fails.

The sizing optimization process to minimize phase noise briefly described above, is adapted in the Algorithm 1 to use DE as the optimization method. For DE, the individuals from the randomly generated population are added to the VCO's netlist and each one of them is simulated. The SPICE simulator is linked within the optimization loop to evaluate the VCO electrical characteristics. From the output *.lis file, the electrical characteristics are extracted to monitor the constraint values, when these are indeed satisfied the solution is considered feasible and the VCO is simulated again with the same individuals. This new simulation features the addition of the necessary commands to execute phase noise simulation to the VCO netlist. Whereas if the constraints are not fulfilled, the solution is unfeasible and then the phase noise, $f(x)$, is set to a high value.

Algorithm 1 DE pseudocode

procedure DE(I_n, $maxGen$, $g(x)$)
    Generate the SPICE netlist of the ring VCO
    for $i = 1 : I_n$ **do**
        Initialize the population randomly and replace the initial individuals (Ws, Ls, V_{ctrl}) into the netlist
        Evaluate the VCO and check the constraints
        if $constraints = 0$ **then**
            Simulate the VCO again and evaluate the objective function
    while $j < maxGen$ **do**
        for $i = 1 : I_n$ **do**
            Create a trial solution from 3 randomly selected parents using (2.1)
            Apply crossover using (2.2)
            Replace the new individual into the netlist
            Simulate the VCO and count the constraints
            if $constraints = 0$ **then**
                Simulate the VCO again and evaluate the objective function
            if the individual's objective function is less than that of the parent **then**
                The new individual replaces the parent using (2.3)

Algorithm 2 PSO pseudocode

procedure PSO(I_n, $maxGen$)
    Generate the SPICE netlist of the ring VCO
    for $i = 1 : I_n$ **do**
        Initialize randomly the particles and replace them (Ws, Ls, V_{ctrl}) into the netlist
        Evaluate the VCO and check the constraints
        if $constraints = 0$ **then**
            Simulate the VCO's phase noise and evaluate the objective function
        Update the p_{best_i} particle considering the constraints and the objective function
        Update the g_{best} particle considering the constraints and the objective function
    for $j = 1 : maxGen$ **do**
        for $i = 1 : I_n$ **do**
            Copy particle i to p
            Update the particle p velocity using (2.4)
            Update the particle p position using (2.5)
            Replace the new particles into the netlist
            Simulate the VCO and count the constraints
            if $constraints = 0$ **then**
                Simulate the VCO's phase noise and evaluate the objective function
            Compare particles i and p
            Update the p_{best_i} particle considering the constraints and the objective function
            Update the g_{best} particle considering the constraints and the objective function

Algorithm 2 [25], shows the transformation of the PSO algorithm for the specific optimization problem of minimizing a ring VCO's phase noise, which means that $g(x) = L\{f_{offset}\}$. Similarly to the process followed with the DE algorithm, with PSO the particles of the randomly generated population are replaced into the VCO's netlist. When the VCO design does not comply with the restrictions, a high value is assigned to the objective function, which is the phase noise. If the VCO does satisfy the constraints, then the phase noise is evaluated. The updating mathematical expressions are given by (2.4) and (2.5).

In PSO the constraint management considers that: when two feasible particles are compared, the particle with the lowest phase noise is selected, if only one of the particles is feasible, then the feasible one is chosen. Lastly, when both particles are not feasible then the particle that complies with more constraints is selected [25].

The limits of the search spaces of the design variables for both DE and PSO algorithms are: $2\ \lambda \leq W \leq 1000\ \lambda$ and $2\ \lambda \leq L \leq 10\ \lambda$ for widths and lengths, respectively, where λ= 90 nm. The control voltage range is set to be from rail-to-rail, $V_{SS} \leq V_{ctrl} \leq V_{DD}$, where $V_{SS} = -0.9\ V$ is the lower supply voltage and $V_{DD} = 0.9\ V$ the higher supply voltage. The frequency and power constraints are set to $f_{min} = 100\ MHz$ and $P_{max} = 30\ mW$, respectively in both algorithms. The optimization with DE and PSO algorithms requires to define a population of I_n individuals or particles, a maximum number of generations *maxGen* and an objective function $g(x)$.

5. Optimization results

DE algorithm executions are carried out setting the number of individuals I_n and amount of generations max_{gen} to 30 and 30 respectively. For the PSO algorithm a population of 60 individuals and a maximum number of generations of 40 are used. The design parameters of each of the 5 best feasible sized solutions for both algorithms as well as the simulated phase noise (PN), frequency and power of the VCO, are summarized in Table 1. For this purpose, the best solutions are considered to be the ones with the lower phase noise.

The phase noise simulation results of the non-optimized design (-93.1 dBc/Hz@1MHz) against the best solution given by the DE (-129.01 dBc/Hz@1MHz) and the PSO (-124.67 dBc/Hz@1MHz) algorithms are shown in Figure 4. The blue signal depicts the original phase noise, whereas the green and orange signals depict the DE and the PSO phase noise, respectively. From Table 1 and Figures 3 and 4 it is noticeable the improvement of 35.91 and 31.57 dBc/Hz@1MHz, with respect to the original design phase noise, for DE and PSO algorithms, respectively. It can be seen that DE algorithm achieved lower phase noise compared to PSO, while requiring less resources to achieve better results. Another point is that compared to DE, PSO required to increase both the population size and the maximum number of generations to 60 and 40, respectively. Additionally, PSO algorithm required approximately two to three times the execution time of DE to generate similar feasible solutions. Finally, to appreciate the usefulness of performing a minimization of phase noise, Table 2 shows a comparison of some relevant parameters in VCO performance of the best sizing result provided by the DE algorithm with other ring VCO topology results in the literature. As one can see, the phase noise performance of the design obtained through optimization with the DE algorithm is comparable to what is already reported in the literature for designs implemented in the same technology and measured at the same offset frequency, while also represents an improvement from the phase noise performance of the non-

optimized design.

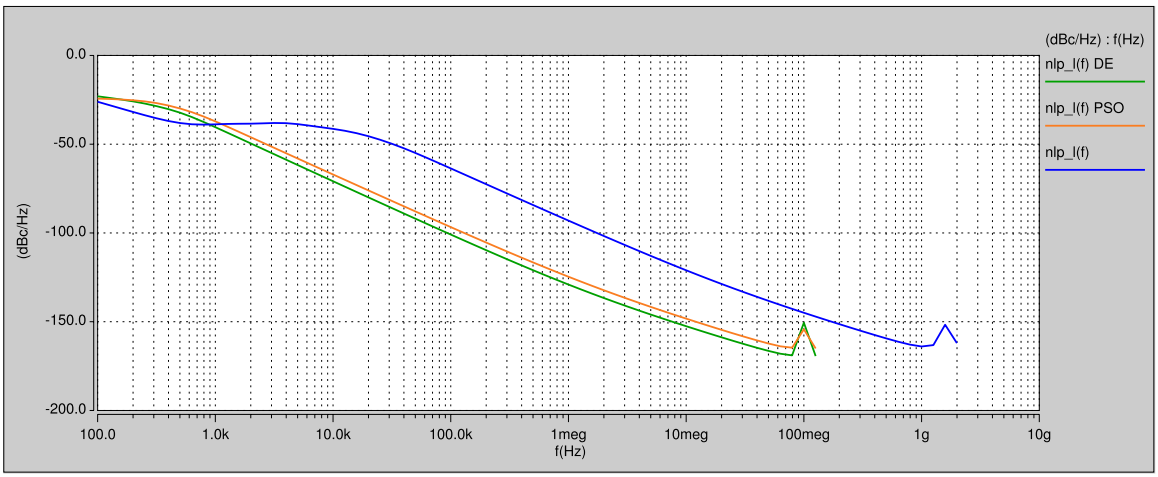


Figure 4. Phase noise of the non-optimized topology (blue) compared to the best sized solutions provided by the DE (green) and PSO (orange) algorithms, given in Table 1.

Table 1. Best 5 feasible sized solution design parameters.

Solution	$W_{MN1}(\mu m)$		$W_{MP1}(\mu m)$		$L_{MN1}(\mu m)$		$L_{MP1}(\mu m)$		$W_{M2}(\mu m)$		V_{ctrl}(V)		Power(mW)		Frequency(MHz)		PN(dBc/Hz@1MHz)	
	DE	PSO	DE	PSO	DE	PSO	DE	PSO	DE	PSO	DE	PSO	DE	PSO	DE	PSO	DE	PSO
1	39.42	20.43	89.1	60.12	0.9	0.72	0.39	0.54	33.3	24.93	-0.9	-0.64	26.41	13.38	101.17	104.58	-129.01	-124.67
2	40.2	13.14	89.95	58.86	0.9	0.54	0.44	0.72	30.79	19.53	-0.88	-0.86	23.52	10.06	100.85	100.69	-128.85	-122.46
3	33.88	7.02	89.25	46.35	0.86	0.81	0.48	0.9	29.37	13.05	-0.7	-0.43	21.57	5.01	100.56	100.38	-128.82	-122.38
4	30.74	31.5	89.4	78.39	0.86	0.63	0.51	0.36	26.88	22.41	-0.69	-0.83	18.47	24.9	100.13	200.87	-128.77	-121.36
5	33.72	23.67	89.27	80.91	0.86	0.81	0.58	0.81	27.41	13.23	-0.77	-0.37	19.32	12.67	100.13	194.4	-128.65	-120.79

Table 2. Ring VCO characteristics compared with similar works.

Work	Tech.(nm)	Topology	Power(mW)	PN($\frac{dBc}{Hz}$)	$\lvert FoM\rvert$ ($\frac{dBc}{Hz}$)	Freq. TR (GHz)	Volt. TR (V)	K_{VCO} ($\frac{GHz}{V}$)
This Work	180	PD	26.41	-129.01@1MHz	-	0.1 to 0.13	-0.9 to -0.2	-
[32]	180	PD	1.06	-138.5@100MHz	-	1.66 to 1.57	1 to 1.4	0.023
[26]	180	SE	0.19	-138@1MHz	-	1 ± 14 %	-	-
[35]	180	SE var.	1.2	-106@1MHz	165.1	0.8 to 1.3	0.5 to 1.6	-
[36]	180	D	28	-92.68@1MHz	-	1.78 to 2.53	$\Delta V = 0.2$	7%
[37]	65	PD	20	-90.08@10.3125GHz	157.34	11 to 2.4	0.1 to 0.75	4.6
[38]	45	SE var.	0.357	-88.54@10MHz	-	41.75 to 0.308	0.2 to 0.7	-
[39]	40	D	1.1	-98.05@1MHz	160.4	0.86 to 1.38	0 to 1.1	-
[40]	28	PD	1.1	-95.7@1MHz	160.7	0.7 to 2.78	-	0.25

6. Conclusions

The optimization of the phase noise performance of an eight stage pseudo-differential CMOS ring VCO through two mono-objective metaheuristics, DE and PSO, was carried out in this paper. Through the optimization process it became noticeable that compared to PSO, the optimization problem was solved more effectively with the DE algorithm, since it gave better results in terms of a lower phase noise while requiring less resources (the problem was solved with a smaller population size and a lower number of maximum generations) and execution time. Also, from the presented results one can see the improvement on phase noise provided by DE and PSO, compared to the preliminary (manual) design.

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Conflict of interest

The authors declare no conflicts of interests.

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