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Research article

Dynamic design and optimization of a power system DC/DC converter using peak current mode control

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Abstract: This paper introduces a control strategy centered on peak current mode (PCM) control within continuous conduction mode (CCM) for regulating the terminal voltage of a constant-power load supplied by a double-inductance buck converter referred to as the "Superbuck". The analysis looks at the converter's dynamic behavior using the State Space Averaging (SSA) technique created by Middlebrook. This dynamic characterization serves the purpose of assessing and ensuring the stability and performance of the system. The suggested control strategy is validated by the experimental and simulation results that are shown, which show a favorable dynamic response and steady-state performance under significant load variations. Practical measurements have demonstrated that the mathematical models accurately predict our converter's dynamic behavior. In addition to its instantaneous response to any voltage change, we also notice that the response in the current mode is faster. In order to examine control stability, the study also includes a temporal analysis of the converter under resistive and resonant load conditions, taking into account different initial voltage conditions. We notice that the time response is a bit slow due to the delays caused by the regulation loop and the output impedance of the converter is high. The Superbuck converter is load-insensitive since it responds without oscillations, just like the output voltage. As a result, PCM has the ability to reduce or even completely eradicate the resonance phenomenon that usually affects these converters' harmonic responses. A compensation ramp is necessary to prevent the double cycle phenomenon, which is the main disadvantage of PCM. The system becomes unstable when duty cycle D surpasses 50%.

Keywords: DC/DC Superbuck converter; characterization; PCM control; mathematical modeling; temporal analysis; stability

1. Introduction

The DC/DC converter holds a crucial role within photovoltaic systems, serving multiple functions including DC power supply, battery charging, and the optimization of power generation by identifying the maximum power point tracking (MPPT) [1,2]. It necessitates a static converter to efficiently adapt the energy from the photovoltaic source to meet the electrical load requirements for effective utilization [3,4].

The dynamic analysis of DC-DC converters traces its roots back to the 1970s, focusing on studying and ensuring system stability and performance. This pursuit has culminated in the development of a canonical model, consisting of a set of parameters capable of describing and predicting the converter's behavior during its operational phase.

By expanding the research outfit to DC/DC and AC/DC converters, as well as hybrid microgrids, this study is part of an increasingly interconnected scientific framework [5,6], where challenges related to stability, efficiency, and energy resilience must be determined to meet the demands of modern energy systems. The results of this research aim to fill serious gaps and provide practical contributions for managing and optimizing converter performance in complex environments.

Considerable progress has been made in control strategies in recent years, particularly by integrating digital innovations and artificial intelligence to improve dynamic stability and energy performance. In particular, methods such as peak current mode control (CMC) and voltage mode control (VMC) have evolved to meet the demands of high-efficiency systems [7–9]. These systems require advanced control arrangements to ensure optimal performance in terms of energy efficiency, stability, and dynamic response.

Among them, current mode control (CMC) has demonstrated an unusual ability to quickly regulate load variations and improve stability in intricate systems. Similarly, voltage mode control (VMC) continues to evolve with the incorporation of digital techniques and algorithms based on artificial intelligence, which offers improved performance in applications with a wide operating range [7]. Similarly, to increase the converters' dynamic response and robustness, type III compensators based on linear matrix inequalities have been created. These developments provide improved build stability and disturbance concealment, which are critical for applications that are sensitive to changes in input pressure and load [7].

On the other hand, new developments like the semiconductors GaN and SiC have made it possible to lower losses and increase power density, which has a direct impact on control decisions [5]. The use of learning standard reinforcement, including through algorithms like proximal policy optimization (PPO), has also been studied for Lift DC/DC converter control.

Control systems that are not only intelligent and adaptive are now possible thanks to artificial intelligence techniques that enable faster reaction times and improved standard compatibility with conventional methods [5].

However, a number of challenges remain in spite of these developments, including maximizing performance in non-linear or perturbation-prone environments and alternating between continuous (CCM) and discontinuous (DCM) conduction modes [7].

Static converters have undergone advancements in their typologies and control methodologies, integrating novel and enhanced techniques, notably voltage mode control (VMC) and current mode control (CMC) as primary control strategies, and other methods [7,10,11]. The selection between these control strategies assumes critical significance in the context of a specific application, taking into account the fundamental principles underlying the chosen control approach and its meaningful impact on the given application's performance [3,4]. The introduction of constraints on the duty cycle in the dynamic model obtained constitutes the means to highlight the case of PCM control. Consequently, PCM makes it possible to reduce and very often even eliminate the effect of the resonance phenomenon, which marks the harmonic responses of these converters controlled by the VMC.

The Superbuck converter, a member of the extensive family of DC/DC converters, is a double-inductor buck chopper that employs peak current mode (PCM) [8] control and operates in continuous conduction mode (CCM) [12–14]. Superconverters, as fourth-order converters, exhibit a resonance phenomenon that presents significant control challenges. The utilization of PCM control offers the advantage of mitigating this resonance effect [15]. However, in PCM control, the duty cycle representing the control current for these converters is the sum of the currents from the two inductors. Consequently, the resonance phenomenon may not be eliminated, as variations in these currents can affect the control characteristics.

Superbuck's SSA-M model under PCM control is established by substituting the constraint on the duty cycle, denoted as $\hat{d}$. In a steady-state condition, the DC components of the converter's electrical parameters (current and voltage) remain constant, except for minor fluctuations caused by the switching frequency and external disturbances, which are typically negligible [15–18]. In dynamic analysis of the converter, disturbances must be considered, leading to the development of a small-signal model. This model allows for a reasonably accurate assessment of the influence of applied disturbances on input and output signals, up to half of the switching frequency.

The investigation proceeds with a comprehensive analysis of the entire system, as depicted in Figure 1, utilizing a set of differential equations to examine the voltage and current behaviors associated with peak current mode (PCM) control. These analyses yield results obtained through simulation employing Matlab. The simulation encompasses two distinct modes of operation: open-loop operation, where the converter operates independently of the output, and closed-loop operation, wherein the converter's control is contingent on the output voltage via feedback control.

The findings affirm the effectiveness of this approach, facilitating precise control of chopper current while mitigating overshoots in various parameters and validating the attenuation of resonances observed in the harmonic response of the system. Notably, the phenomenon of the double cycle associated with PCM when the duty cycle (D) exceeds 50% is observed and thoroughly investigated, including an examination of the impact of compensation ramp on the system's behavior.

Advances in Superbuck converter control strategies are focused on improving stability, energy efficiency, and performance under various load conditions. The incorporation of techniques such as PCM, ramp compensation, and adaptive control is making significant contributions to overcoming existing limitations. These innovations make super buck converters more robust, reliable, and efficient, paving the way for increasingly complex applications, particularly in hybrid and renewable energy systems.

Stability and noise sensitivity issues are often exacerbated in some key DC/DC converter requirements, particularly in demanding applications such as renewable energy systems, hybrid microgrids, or floating dynamic loads, where high duty cycles lead to instability as switch conduction

times become very short, which can disrupt current and voltage regulation. Alternatively, converters powered by sources of (electromagnetic) noise or connected to complex systems such as hybrid microgrids may experience performance degradation. Alternatively, rapid changes in load or input voltage can make the system unstable if control strategies are not vigorous.

In addition to the compensation ramp. We add an active filter (inductor or capacitor) to attenuate the noise before it influences the control signals and implement a predictive control algorithm that adjusts the parameters of the DC/DC converter.

The latter part of the study centers on the practical implementation of the research, encompassing the fabrication of a prototype comprising a Superbuck converter representing the power board and a control board featuring a Microchip family microcontroller. Experimental measurements are conducted on this practical prototype to corroborate the theoretical analyses.

The study presented here, as illustrated in Figure 1, will first detail the operating principle of the DC/DC Superbuck converter while presenting the electrical circuit, leading to its dynamic modeling in CCM mode through the application of the SSA_M method. The introduction of constraints on the duty cycle D in the obtained dynamic model. We will present the waveform of the inductor current of the PCM-controlled chopper, where we have highlighted the double cycle phenomenon for an application with D > 50%, which requires the addition of an artificial ramp for compensation with a slope whose value must be calculated precisely for good compensation; otherwise, when a slope equal to 0, this instability phenomenon is inevitable.

This will be introductory to the correction of the system's performance. We will also address the temporal analysis of the complete system represented by differential equations in order to observe the behavior of voltages and currents with results obtained through simulation, and then we will examine the closed-loop system to study its stability and anticipate a guaranteed controller. The third part is dedicated to the validation of the mathematical model of the Superbuck converter and the experimental measurements carried out on a practical prototype. A comprehensive investigation involving both simulation and prototype development of the Superbuck converter was conducted with dual objectives: to derive a mathematical model and to facilitate a comparative analysis, enabling the selection of an optimal control strategy tailored to the specific application, thus harnessing its inherent benefits.

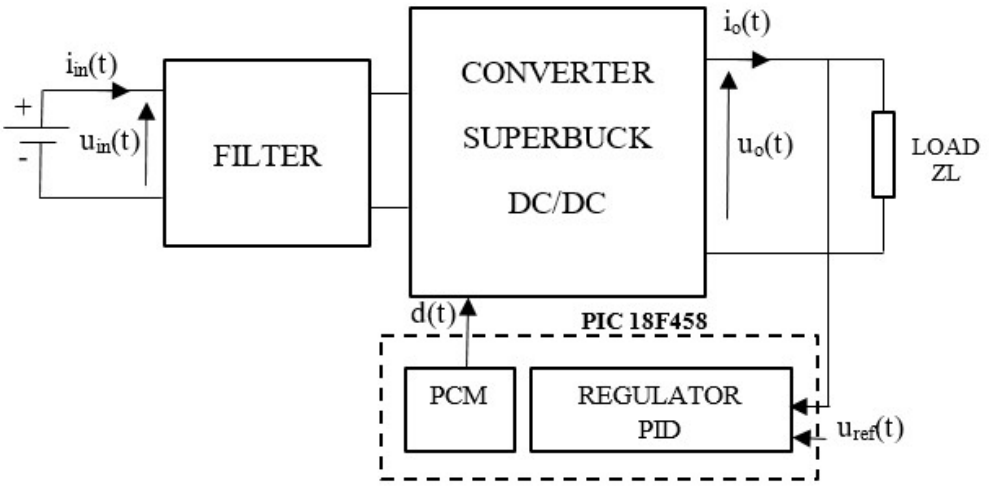

Figure 1. The implemented system configuration.

2. Research materials and experimental procedures

2.1. Analysis and modeling of DC-DC converter systems sub-subheading

2.1.1. Analysis of DC-DC converter

The Superbuck represents a double-inductance step-down converter serving as the primary power source for the circuit's functionality. Its operational characteristics are elucidated through rigorous circuit analysis, as documented in references [19–23]. The converter's operation unfolds in two distinct phases, contingent upon the state of the switching mechanism, as illustrated in Figure 2 during the Switching frequency f_s.

Inductors and capacitors are modeled in consideration of their esr (equivalent series resistance): r_{Li} & r_{Ci}.

The power transistor is modeled, to simplify it, as being a switch with only its series resistance in the 'ON' state: rds.

The diode is modeled by an inverse voltage source in series with its equivalent resistance, U_D & r_d.

The source is considered to be an ideal voltage source with a value of U_{in}.

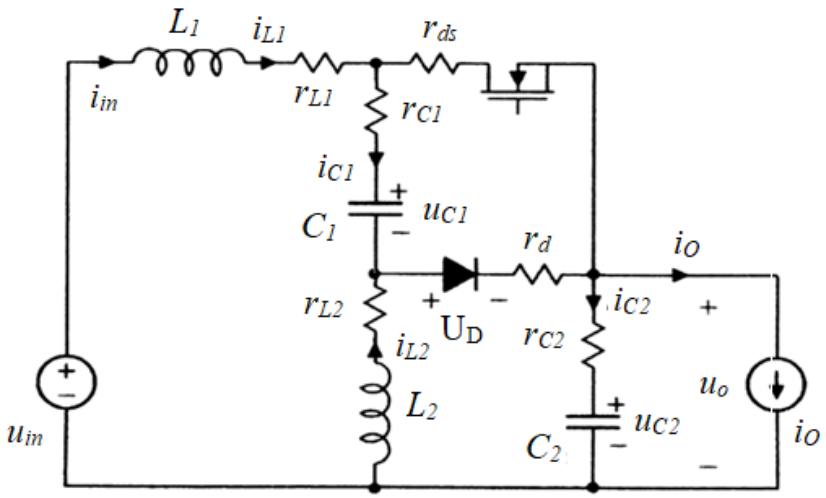

Figure 2. The electric circuit configuration of the Superbuck converter.

Q: MOSFET transistor

During the 'ON' state, characterized by the closure of switch Q, the current in inductor L_1, situated in series with the generator, experiences an increment, resulting in the accumulation of magnetic energy. This increase in current also propagates through inductor L_2. Subsequently, the current denoted as 'i_{L1}', flows through capacitor C_2 and the load.

For $\boldsymbol{T_{on}}$: $\boldsymbol{0 < t < dT_s}$:

$$u_{L1}(t) = L_1\frac{di(t)}{d(t)} = -(r_{L1} + r_{ds} + r_{C2})\, i_{L1} - (r_{ds} + r_{C2})\, i_{L2} - u_{C2} + u_{in} + r_{C2}i_o, \quad (1)$$

$$u_{L2}(t) = L_2\frac{di(t)}{d(t)} = -(r_{ds} + r_{C2})\, i_{L1} - (r_{L2} + r_{ds} + r_{C1} + r_{C2})\, i_{L2} + u_{C1} - u_{C2} + r_{C2}i_o, \quad (2)$$

$$i_{C1}(t) = C_1\frac{du(t)}{d(t)} = -i_{L2}, \tag{3}$$

$$i_{C2}(t) = C_2\frac{du(t)}{d(t)} = i_{L1} + i_{L2} - i_o, \tag{4}$$

$$i_{in}(t) = i_{L1}, \tag{5}$$

$$u_o(t) = r_{C2}\, i_{L1} + r_{C2}\, i_{L2} + u_{C2} - r_{C2}i_o. \tag{6}$$

In the 'OFF' state, denoted by the open position of switch Q and the concurrent activation of the diode, the inductance L_1, positioned in series with capacitor C_1 and the diode, contributes to the continued accumulation of energy from the previous phase. Consequently, this accumulated current flows through capacitor C_2. The modulation of the cyclical relationship 'd' is employed to adjust the release of stored energy. The presence of inductances facilitates the controlled discharge of current from the power source. Furthermore, the inclusion of capacitor C2 serves to regulate and limit the output ripple voltage.

For$\boldsymbol{T_{off}}$: $\boldsymbol{dT_s < t < T_s}$:

$$u_{L1}(t) = L_1\frac{di(t)}{d(t)} = -(r_{L1} + r_{C1} + r_d + r_{C2})\, i_{L1} - (r_d + r_{C2})i_{L2} - u_{C1} - u_{C2} - u_D + u_{in} + r_{C2}i_o, \tag{7}$$

$$u_{L2}(t) = L_2\frac{di(t)}{d(t)} = -(r_d + r_{C2})\, i_{L1} - (r_{L2} + r_d + r_{C2})i_{L2} - u_{C2} + r_{C2}i_0 - u_D, \tag{8}$$

$$i_{C1}(t) = C_1\frac{du(t)}{d(t)} = i_{L1}, \tag{9}$$

$$i_{C2}(t) = C_2\frac{du(t)}{d(t)} = i_{L1} + i_{L2} - i_o, \tag{10}$$

$$i_{in}(t) = i_{L1}, \tag{11}$$

$$u_o(t) = r_{C2}i_{L1} + r_{C2}i_{L2} + u_{C2} - r_{C2}i_o. \tag{12}$$

Then, over a switching period on Ts:

In the subsequent interval spanning the 'ON' state duration, denoted as the switching period 'Ts':

Inductance voltages:

$$\begin{aligned} L_1 di(t)/d(t) = {} & [-(r_{L1} + r_{ds} + r_{C2})i_{L1} - (r_{ds} + r_{C2})i_{L2} - u_{C2} + u_{in} + r_{C2}i_0]d \\ & + [-(r_{L1} + r_{C1} + r_d + r_{C2})i_{L1} - (r_d + r_{C2})i_{L2} - u_{C1} - u_{C2} - u_D + u_{in} + r_{C2}i_0]d', \end{aligned} \tag{13}$$

$$\begin{aligned} \frac{dil1(t)}{d(t)} = {} & \frac{1}{L1}[-(r_{L1} + r_{ds} + dr_{ds} + d'(r_{C1} + r_d))i_{L1} \\ & - (r_{C2} + dr_{ds} + d'r_d)i_{L2} - d'u_{C1} - u_{C2} - d'u_D + u_{in} + r_{C2}i_0], \end{aligned} \tag{14}$$

$$\begin{aligned} L_2\frac{dil2(t)}{d(t)} = {} & [-(r_{ds} + r_{C2})i_{L1} - (r_{L2} + r_{ds} + r_{C1} + r_{C2})i_{L2} + u_{C1} - u_{c2} + r_{C2}i_0]d \\ & + [-(r_d + r_{C2})i_{L1} - (r_{L2} + r_d + r_{C2})i_{L2} - u_{C2} + r_{C2}i_0 - u_D]d', \end{aligned} \tag{15}$$

$$\frac{dil2(t)}{d(t)} = \frac{1}{L2}[-(r_{L2} + r_{ds}d + d'r_d)i_{L1} - [r_{L2} + r_{C2} + (r_{ds} + r_{L1})d + r_d d']i_{L2} + du_{C1} - u_{C2} - d'u_D + r_{C2}i_0], \quad (16)$$

where: $(d' = 1 - d)$.

Capacitor currents:

$$i_{C1}(t) = C_1\frac{duc1(t)}{d(t)} = -i_{L2}d + i_{L1}d', \quad (17)$$

$$\frac{duc1(t)}{d(t)} = \frac{1}{C1}(-i_{L2}d) + \frac{1}{C1}i_{L1}d', \quad (18)$$

$$i_{C2}(t) = C_2\frac{duc2(t)}{d(t)} = [i_{L1} + i_{L2} - i_0]d + [i_{L1} + i_{L2} - i_0]d', \quad (19)$$

$$\frac{duc2(t)}{d(t)} = \frac{1}{C1}[i_{L1} + i_{L2} - i_0]d + \frac{1}{C1}[i_{L1} + i_{L2} - i_0]d', \quad (20)$$

$$u_0 = u_{C2} + r_{C2}C_2\frac{duc2(t)}{d(t)} = u_{C2} + r_{C2}(i_{L1} + i_{L2} - i_0), \quad (21)$$

$$i_{in} = i_{L1}. \quad (22)$$

- Principal relationships and constraints governing components in the steady-state regime

a. Determination of the resting point

The aim of this analysis is to establish the fundamental correlations between the average values of inductance currents and input currents, as well as capacitance voltages and output voltages. These correlations define the operational characteristics of the circuit in its quiescent state. It is important to note that under steady-state conditions, the current flowing through a capacitor and the voltage across an inductor demonstrate periodic behaviors with mean values of zero.

- The average voltage across inductance is zero: <u_L> = 0.
- The average current within capacitor C is zero: <i_C> = 0.

Capacitor voltages:

$$U_{C2} = U_0, \quad (23)$$

$$U_{C1} = Uin - (Dr_{L1} - D'r_{L2})I_0. \quad (24)$$

Con:

$$U_0 = DU_{in} - D'U_D - (Dr_{ds} + DD'r_{C1} + D'r_d + D^2r_{L1} + D'^2r_{L2})I_0. \quad (25)$$

Inductance currents:

$$I_{L1} = DI_0, \quad (26)$$

$$I_{L2} = D'I_0, \quad (27)$$

$$D'I_{L1} = DI_{L2}, \quad (28)$$

$$I_{in} = I_{L1}. \quad (29)$$

b. Current ripples

The determination of the current ripple of a DC/DC converter is derived from its voltage and current equations during its steady-state operation. Its solution can be succinctly expressed as Eq (30), as referenced in [12,13].

$$\Delta i_L = dd' \frac{Ts}{2} \sum_{i=1}^{n} (m_{i1} + m_{i2}) \tag{30}$$

To elaborate on this further:
n: represents the number of inductances integrated into the circuit.
m_{i1} and m_{i2} denote the rising and falling slopes characterizing the current of each individual inductor.

In the absence of disturbances and under the operation of the converter at its resting point state, the description of this ripple is encapsulated in Eq (31):

$$\Delta i_L = DD' \frac{T_s}{2} (M_1 + M_2). \tag{31}$$

In the context of this investigation, our focus lies on the oscillatory behavior exhibited by the input current, denoted as $i_L(t)$, as it passes through the switch Q and the diode. This behavior is formally defined as follows:

$$i_L = i_{L1} + i_{L2}. \tag{32}$$

The determination of the inductance ripple current in the Superbuck converter is derived through the utilization of Eq (30), while the relevant parameters are ascertained from Eqs (33)–(36). This coherent methodology results in the following relationship:

$$m_{11} = \frac{1}{L_1}[-(r_{L1} + r_{ds} + r_{C2}) i_{L1} - (r_{ds} + r_{C2}) i_{L2} - u_{C2} + u_{in} + r_{C2} i_0], \tag{33}$$

$$m_{12} = -\frac{1}{L_1}[-(r_{L1} + r_{C1} + r_d + r_{C2}) i_{L1} - (r_d + r_{C2}) i_{L2} - u_{C1} - u_{C2} - u_D + u_{in} + r_{C2} i_0], \tag{34}$$

$$m_{21} = \frac{1}{L_2}[-(r_{ds} + r_{C2}) i_{L1} - (r_{L2} + r_{ds} + r_{C1} + r_{C2}) i_{L2} + u_{C1} - u_{C2} + r_{C2} i_0], \tag{35}$$

$$m_{22} = -\frac{1}{L_2}[-(r_d + r_{C2}) i_{L1} - (r_{L2} + r_d + r_{C2}) i_{L2} - u_{C2} + r_{C2} i_0 - u_D]. \tag{36}$$

Incorporating these equations into Eq (30) yields the following result, as documented in reference [12]:

$$< i_{L1}(t) > + < i_{L2}(t) > = < i_{CO}(t) > - m_C dT - \Delta i_L, \tag{37}$$

$$\Delta i_L = dd' \frac{Ts}{2} \left(\frac{< u_1 >}{L_1} + \frac{< u_2 >}{L_2} \right). \tag{38}$$

Such as:

$$< u_1 > = < u_{C1} > + U_D + (r_{C1} + r_d - r_{ds}) < i_{L1} > + (r_d - r_{ds}) < i_{L2} >, \tag{39}$$

$$< u_2 > = < u_{C1} > + U_D + (r_d - r_{ds}) < i_{L1} > + (r_d - r_{ds} - r_{C1}) < i_{L2} >. \tag{40}$$

Through the substitution of the variables within this equation with their pre-defined values established for static operational conditions, we arrive at the following expression:

$$\Delta i_L = DD' \frac{Ts}{2} \left(\frac{U1}{L_1} + \frac{U2}{L_2} \right). \tag{41}$$

Such as:

$$U1 = -\frac{DI_o(r_{L1}+r_{ds}) + D'(I_o r_{ds} - U_{in})}{D'^2}, \tag{42}$$

$$U2 = -\frac{DI_o(r_{L1}+r_{ds}) + D'(I_o(r_{ds}+r_{C1}) - U_{in})}{D'^2}. \tag{43}$$

The term U1 defines the part of the current i_{L1}, and the term U2 defines the part of the current i_{L2} when we replace all the data in Eq (31).

The motivation behind the analysis of this ripple current is to enable the assessment of the upper limit of current that the power transistor in the Superbuck converter can endure. In pursuit of this objective, the maximum ripple current is ascertained by equating Eq (44) to zero and subsequently solving for the duty cycle variable, denoted as D. This procedure allows us to determine the maximum allowable ripple current (Δi_Lmax) associated with a given duty cycle ($D\_\Delta i_{Lmax}$).

The differentiation of Eq (41) in relation to the variable D results in the following expression:

$$\frac{d\Delta iL}{dD} = -\frac{1}{2f_s D'} * \left(\frac{D-D'}{D'} X - DY \right), \tag{44}$$

where

$$X = DA\left(\frac{1}{L_1} + \frac{1}{L_2}\right) + D'\left(\frac{B}{L_1} + \frac{C}{L_2}\right), \tag{45}$$

$$Y = A\left(\frac{1}{L_1} + \frac{1}{L_2}\right) - \frac{B}{L_1} - \frac{C}{L_2}, \tag{46}$$

$$A = I_o * (r_{L1} + r_{ds}), \tag{47}$$

$$B = I_o * r_{ds} - U_{in}, \tag{48}$$

$$C = I_o * (r_{C1} + r_{ds}) - U_{in}. \tag{49}$$

Consequently, the Superbuck's power transistor can be chosen according to the peak value of its current I_{in_p} from Eq (50):

$$I_{in\_p} = I_{in} + \Delta i_{in} = \frac{I_o}{D'} + \Delta i_{in}. \tag{50}$$

Therefore, the maximum value that this current can reach is such that:

$$I_{in\_p\_max} = I_{in\_max} + \Delta i_{in\_max} = \frac{I_{o\_max}}{D'_{\Delta i_{in\_max}}} + \Delta i_{in\_max}. \tag{51}$$

The evolution of this ripple as a function of the duty cycle shows that it increases as D increases until it reaches its maximum value described by Eq (44) and then falls very rapidly beyond this

maximum point. The effect of parasitic elements (esr) is very noticeable on the current ripple curve in Figure 3, where the values reached by the latter are very different when esr are taken into account. This means that their inclusion in the model enables us to estimate the exact value of the ripple rate.

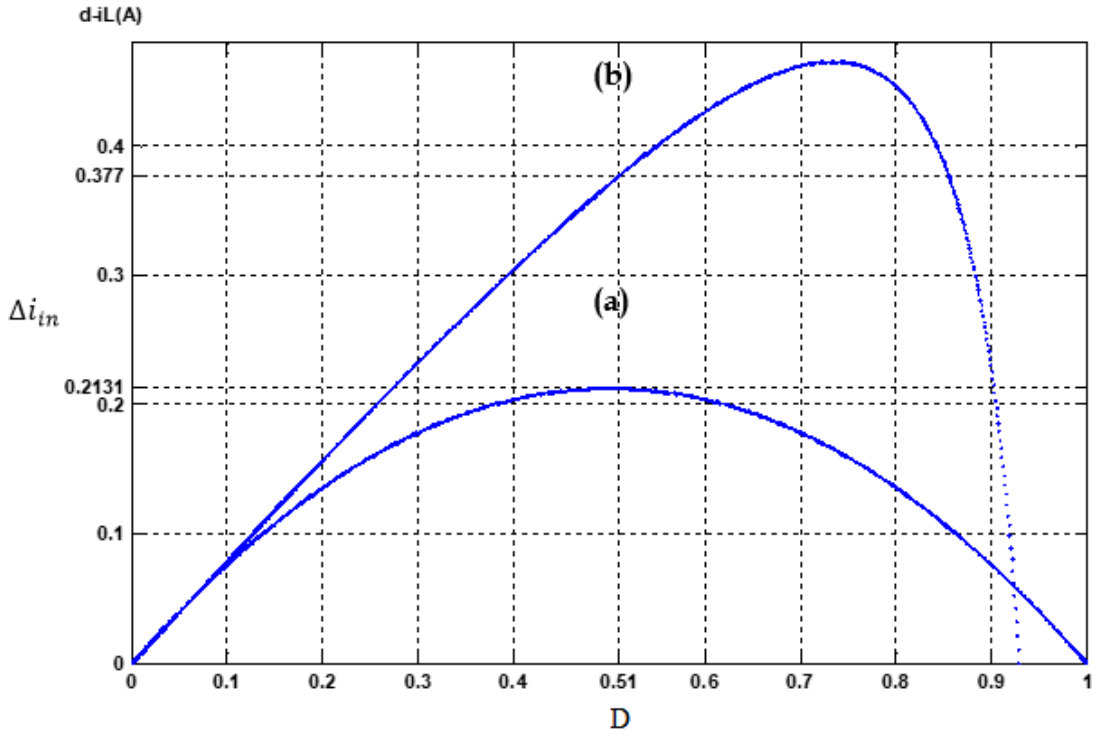

Figure 3. Current ripple shape as i_{in} function of D of the Superbuck converter operating in continuous conduction mode. (a) Ideal curve without esr. (b) Real curve with esr.

2.1.2. Application of peak current mode (PCM) modeling to the Superbuck converter

- PCM control

Superconverters are acknowledged as fourth-order converters, distinguished by a resonance phenomenon that poses challenges for their control. The implementation of peak current mode control (PCM) offers the benefit of mitigating this resonance, as demonstrated in reference [15]. Nevertheless, the PCM control current pertaining to the duty cycle in these converters is comprised of the summation of currents associated with two inductors. This composition accounts for the persistence of the resonance phenomenon to some extent, as variations in these distinct currents can undermine the efficacy of the control paradigm depicted in Figure 4, as discussed in references [24–26].

As a consequence, the duty cycle constraint 'd' takes the form of Eq (53) as described in the following references [27,28]. The primary aim is to ascertain its various coefficients.

$$\hat{d}(t) = f(\hat{\imath}_{CO},\ \hat{\imath}_{L1},\ \hat{\imath}_{L2},\ \hat{u}_{C1},\ \hat{u}_{C2},\ \hat{u}_{in},\ \hat{\imath}_{O},\ t) \tag{52}$$

$$\hat{d} = F_m(\hat{\imath}_{CO} - q_{L1}\hat{\imath}_{L1} - q_{L2}\hat{\imath}_{L2} - q_{C1}\hat{u}_{C1} - q_{C2}\hat{u}_{C2} - q_{in}\hat{u}_{in} - q_o\hat{\imath}_o) \tag{53}$$

The switch control mechanism is achieved by comparing the current 'iin(t)' with 'ico(t)' as depicted in Figure 5, allowing for the computation of the current 'iin(t)' average value.

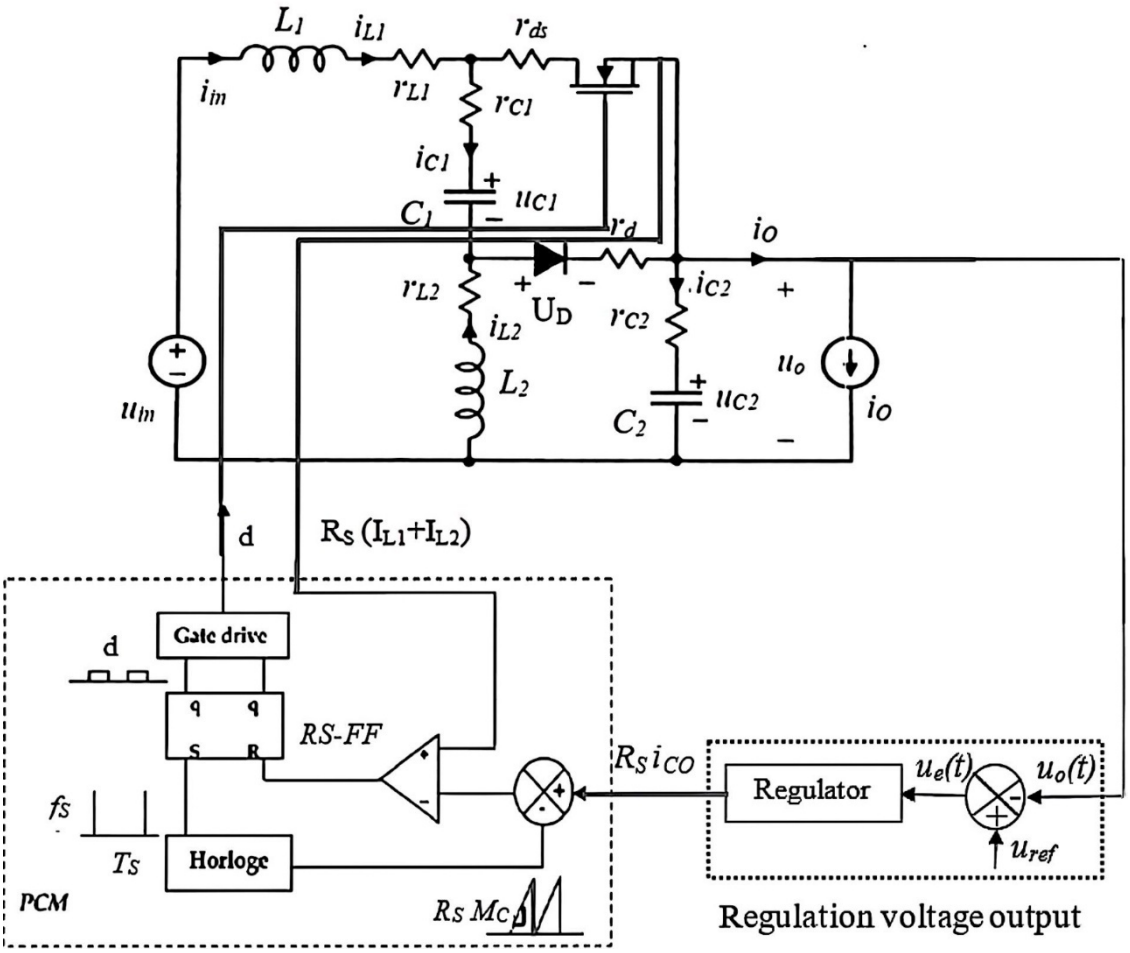

Figure 4. Superbuck converter controlled by PCM.

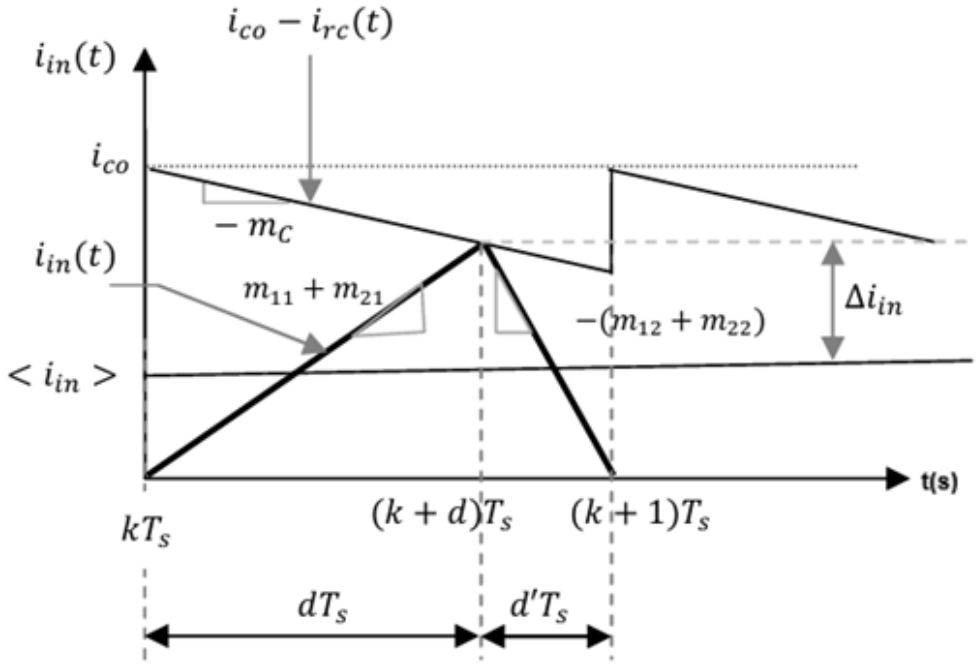

Figure 5. Current shape of the inductors at the comparator.

$$i_{in}(t) = i_{L1}(t) + i_{L2}(t) \tag{54}$$

$$< i_{in}(t) \geq < i_{L1}(t) > \ + < i_{L2}(t) > = < i_{CO}(t) > - m_C dT - \Delta i_L \tag{55}$$

With the exception of the compensation ramp ($\widehat{m}_C = M_C$), all signals within Eq (55) are subject to disturbances, including the slopes 'm_ij'.

$$i_{L1}(t) = I_{L1} + \hat{\imath}_{L1}(t) \tag{56}$$

$$i_{L2}(t) = I_{L2} + \hat{\imath}_{L2}(t) \tag{57}$$

$$i_{CO}(t) = I_{CO} + \hat{\imath}_{CO}(t) \tag{58}$$

$$d(t) = D + \hat{d}(t) \tag{59}$$

$$m_{11}(t) = M_{11} + \widehat{m}_{11}(t) \tag{60}$$

$$m_{12}(t) = M_{12} + \widehat{m}_{12}(t) \tag{61}$$

$$m_{21}(t) = M_{21} + \widehat{m}_{21}(t) \tag{62}$$

$$m_{22}(t) = M_{22} + \widehat{m}_{22}(t) \tag{63}$$

$$\Delta i_L = \frac{dd'T}{2}\sum_{i=1}^{n}(m_{i1} + m_{i2}) = \frac{dd'T_s}{2}\left(\frac{<u1>}{L_1} + \frac{<u2>}{L_2}\right) \tag{64}$$

The introduction of Eqs (56)–(63) into (64) and into (55) thereafter results in an equation with four terms:

A static component: Corresponds to the static state of the converter.

First-order term: This is the linear part of the circuit characteristic, located in the low frequencies, and is the desired term.

Second and 3rd order terms: These are non-linear components of very low amplitudes obtained by the product between the different AC components, which is negligible in this case. Therefore, we obtain

$$\hat{\imath}_{L1} + \hat{\imath}_{L2} = \hat{\imath}_{CO} - \left[M_C T_s + (D' - D)\frac{T_s}{2}\left(\frac{U_1}{L_1} - \frac{U_2}{L_2}\right)\right]\hat{d} - DD'\frac{T_s}{2}.\left[\left(\frac{1}{L_1} + \frac{1}{L_2}\right)\hat{u}_{C1} + \left(\frac{R_{q1}}{L_1} + \frac{R_{q2}}{L_2}\right)\hat{\imath}_{L1} + \left(\frac{R_{q2}}{L_1} + \frac{R_{q3}}{L_2}\right)\hat{\imath}_{L2}\right]. \tag{65}$$

The solution for Eq (65) in terms of '$\hat{d}$' can be expressed in the form of Eqs (54) and (55), as follows:

$$R_{q1} = r_{C1} + r_d - r_{ds},$$

$$R_{q2} = r_d - r_{ds},$$

$$R_{q3} = r_d - r_{C1} - r_{ds}.$$

The dynamic small-signal model establishes the state representation of the converter when the internal control loop of current through the PCM is established in continuous conduction mode (CCM) in Figure 6.

$$\begin{bmatrix} \frac{d\hat{\imath}_{L1}}{dt} \\ \frac{d\hat{\imath}_{L2}}{dt} \\ \frac{d\hat{u}_{C1}}{dt} \\ \frac{d\hat{u}_{C2}}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{R_1 + F_m\, q_{L1} U_1}{L_1} & -\frac{R_2 + F_m\, q_{L2} U_1}{L_1} & -\frac{\dot{D} + F_m\, q_{C1} U_1}{L_1} & -\frac{1}{L_1} \\ -\frac{R_2 + F_m\, q_{L1} U_2}{L_2} & -\frac{R_3 + F_m\, q_{L2} U_2}{L_2} & \frac{D - F_m\, q_{C1} U_2}{L_2} & -\frac{1}{L2} \\ \frac{\dot{D} + F_m\, q_{L1} I_0}{C_1} & -\frac{D - F_m\, q_{L2} I_0}{C_1} & \frac{F_m\, q_{C1} I_0}{C_1} & 0 \\ \frac{1}{C_2} & \frac{1}{C_2} & 0 & 0 \end{bmatrix} \begin{bmatrix} \hat{\imath}_{L1} \\ \hat{\imath}_{L2} \\ \hat{u}_{C1} \\ \hat{u}_{C2} \end{bmatrix}$$

$$+ \begin{bmatrix} \frac{1}{L_1} & \frac{r_{C2}}{L_2} & F_m \frac{U_1}{L_1} \\ 0 & \frac{r_{C2}}{L_2} & F_m \frac{U_2}{L_2} \\ 0 & 0 & -F_m \frac{I_0}{C_1} \\ 0 & -\frac{1}{C_2} & 0 \end{bmatrix} \begin{bmatrix} \hat{u}_{in} \\ \hat{\imath}_o \\ \hat{\imath}_{co} \end{bmatrix}$$

$$\begin{bmatrix} \hat{\imath}_{in} \\ \hat{u}_o \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & M \end{bmatrix} \begin{bmatrix} \hat{\imath}_{L1} \\ \hat{\imath}_{L2} \\ \hat{u}_{C1} \\ \hat{u}_{C2} \end{bmatrix} + \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} \hat{u}_{in} \\ \hat{\imath}_o \\ \hat{\imath}_{co} \end{bmatrix}$$

Figure 6. The dynamic small-signal model of the converter.

- Maximum duty cycle Dmax

In order to maintain the stability of the current loop, it is imperative to secure a finite and positive value for the coefficient, thus preserving the finite nature of the negative feedback loop as referenced in [7]. Consequently, there arises the need to ascertain the specific threshold value at which the coefficient may attain infinity.

$$F_m \to \infty \Rightarrow T_S M_c + \frac{(D'_{min} - D_{max}) T_S}{2} \left(\frac{U_1}{L_1} + \frac{U_2}{L_2}\right) = 0 \tag{66}$$

The solution of this equation concerning the variable D is characterized by the following:

$$D_{max} = 0.5 + \frac{L_1 L_2 M_c}{L_1 U_2 + L_2 U_1}. \tag{67}$$

Hence, to ensure that Fm remains positively finite, it is necessary that

$$D < D_{max} \ \text{(or: } D' > D'_{min}).$$

- Mc compensation ramp

In peak current mode control (PCM), the inclusion of the Mc compensatory ramp is a necessary measure to maintain the stability of the converter, particularly when the duty cycle (D) exceeds 50%.

We have established specific criteria for determining the value of Mc. In our particular scenario, we will employ the formula for Dmax under the condition where F_m approaches infinity, as outlined in references [12,25,29]. This approach enables the sizing of Mc for the most challenging scenario, ensuring its efficacy even when Dmax reaches 100%.

$$D_{max} = 0.5 + \frac{L_1 L_2 M_c}{L_1 U_2 + L_2 U_1} = 1 \tag{68}$$

$$\Rightarrow M_c = \frac{1}{2}\left(\frac{U_1}{L_1} + \frac{U_2}{L_2}\right) \tag{69}$$

This represents the requisite value for the compensatory ramp to achieve effective compensation. Therefore, when the value of F_m is equated to:

$$F_m = \frac{1}{D'T_s\left(\frac{U_1}{L_1} + \frac{U_2}{L_2}\right)}. \tag{70}$$

In these circumstances, the selection of Fm will meet the requirement for ensuring the stability of the internal current loop.

The subsequent analysis was conducted on a Superbuck converter supplied with a 20 V input voltage and aimed at achieving a 10 V output voltage. The relevant circuit components and their values are presented in Table 1 as follows:

Table 1. Values of the components employed in the investigation of the Superbuck converter.

Parameter	Symbol	Value
Voltage source	Uin	20 V
Voltage across the load	Uo	10 V
Current load	Io	2.5 A
Inductor 1	L_1	15 µH
Series resistance of L_1	r_{L1}	80 mΩ
Inductor 2	L_2	15 µH
Series resistance of L_2	r_{L2}	55 mΩ
Capacitor 1	C_1	20 µF
Series resistance of C_1	r_{C1}	100 mΩ
Capacitor 2	C_2	25 µF
Series resistance of C_2	r_{C2}	10 mΩ
Diode voltage (BY30F)	U_D	0.3 V
Diode resistance	r_d	50 mΩ
Resistance on the MOSFET (IRF740)	r_{ds}	0.25 Ω
Switching frequency	f_s	440 KHz
Switching period	$Ts = 1/f_s$	2.27 µs
Load resistance	R_L	4 Ω

2.2. Simulation results

The temporal analysis of the Superbuck converter involves the examination of its response over

time, encompassing both current and voltage waveforms. This analysis is conducted using SIMULINK, an extension of MATLAB renowned for its graphical representation of mathematical functions and systems through block diagrams.

Figure 7 illustrates the overall structure of the converter model, based on the derived state equations. The converter block is configured as a quadruple, subject to an input vector (u_{in}, i_o, d) representing the control signals, which in turn yields the output vector (i_{in}, u_o).

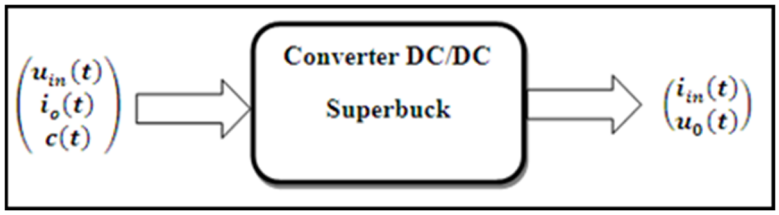

Figure 7. Generic quadruple representation of a Superbuck DC-DC converter.

This quadruple's internal structure is established through equations that describe the various signals within the circuit, as depicted in Figure 8. The block is further subdivided into sub-blocks, each corresponding to an equation that defines its output. Consequently, a model is constructed in which the primary parameters exchanged among these structures are voltages and currents. This model's form is presented in Figure 8, enabling the observation of state vector waveforms, x(t), and output vector waveforms, u(t), provided by their respective outputs.

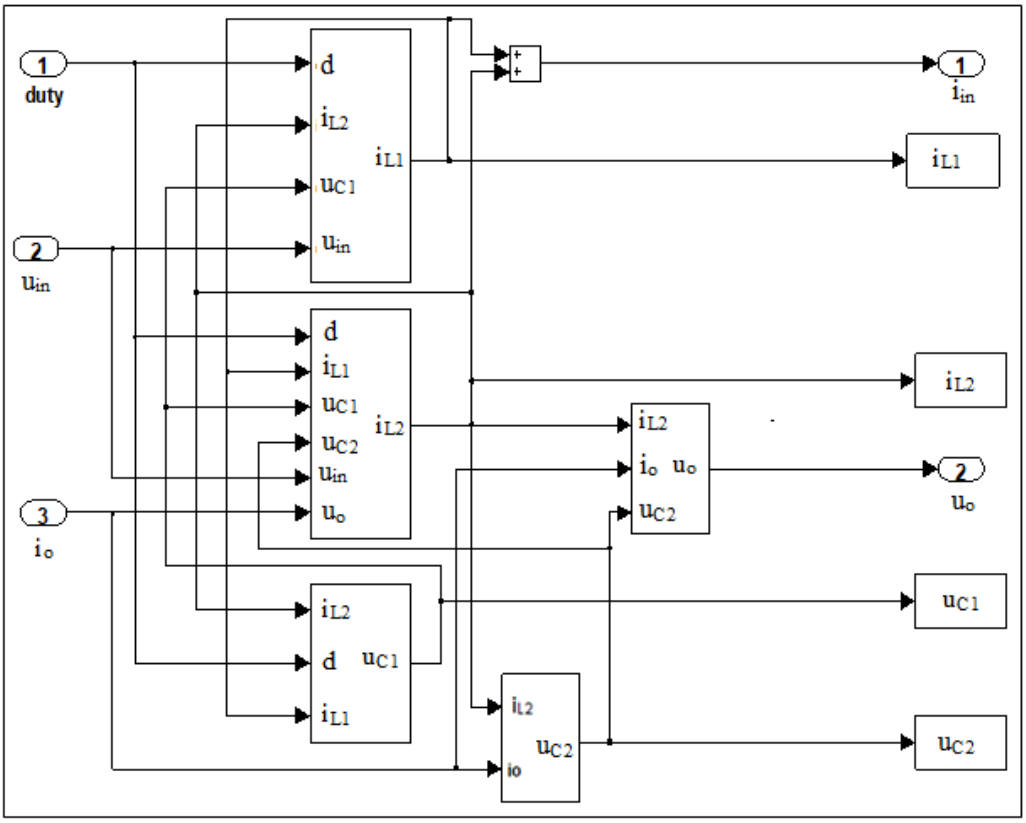

Figure 8. Illustration of the internal structure of the Superbuck converter at mean values.

2.2.1. Implementing an open-loop control mechanism for the Superbuck power converter managed by a peak current mode (PCM) system

The objective behind utilizing a temporal representation of the system dynamics within voltage mode control (VMC) is to enhance peak current mode (PCM) control by modifying the control block, as depicted in Figure 9. The output voltage remains unaltered to facilitate the observation of the converter's response.

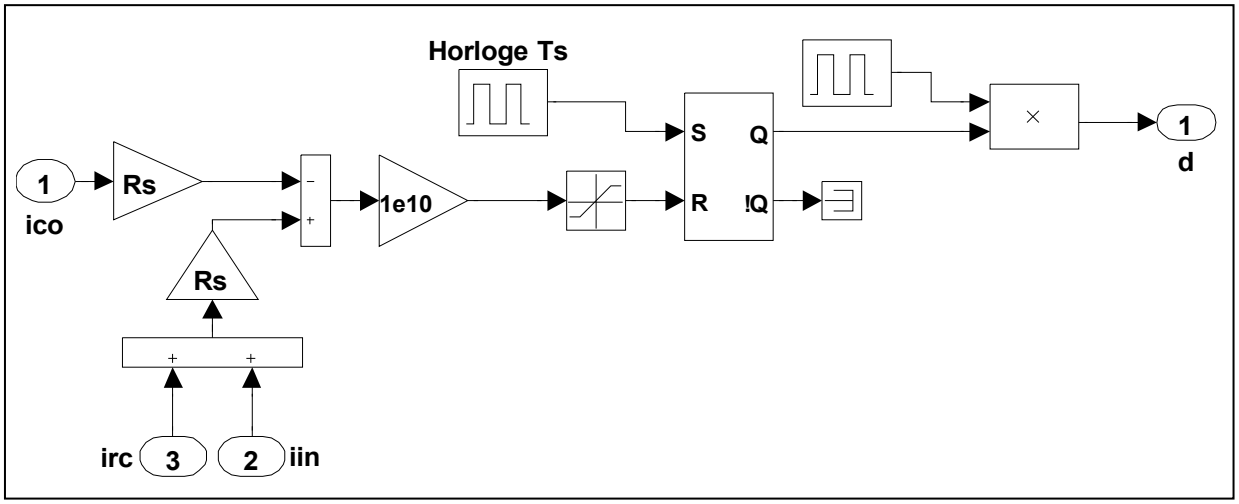

Figure 9. An illustrative diagram depicting the PCM control generator.

The internal configuration of the peak current mode (PCM) control block is derived from the dynamic model depicted in Figure 8. This model involves a comparison between the control current $\boldsymbol{i_{co}}$ and a compensatory ramp $\boldsymbol{i_{rc}}$. The compensatory ramp takes the form of a saw tooth signal with a chopping period T_s to ensure synchronization with the clock frequency. This choice is made such that a double cycle cannot occur for duty cycles (D) equal to or exceeding 50%.

Through ongoing analysis, we have determined the optimal value for the worst-case scenario (D = 100%). The resulting ramp manifests as a saw tooth signal with a period T_s, designed to match the clock frequency precisely, as illustrated in Figure 10. The waveform is generated using the equation provided in Eq (71).

$$i_{rc}(t) = M_c t \tag{71}$$

With:

$$M_c = \frac{1}{2}\left(\frac{U_1}{L_1} + \frac{U_2}{L_2}\right) \tag{72}$$

By employing the comparator equation in conjunction with the characteristics of the ramp and the switch current, it becomes possible to compute the requisite reference current value.

$$i_{co}(t) = i_{in}(t) + i_{rc}(t) \tag{73}$$

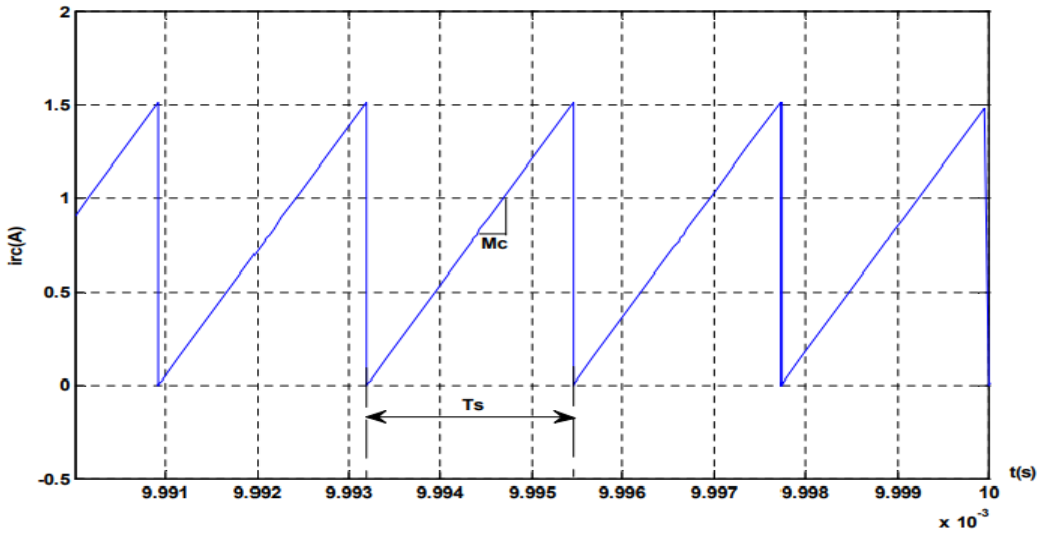

Figure 10. Waveform of the compensation ramp.

The current pattern at the comparator, which contributes to this phenomenon, is depicted in Figure 11. By performing a numerical calculation based on the preceding equation, it is possible to determine the specific value for this set point. Notably, the slope of the compensation ramp corresponds precisely to the downward slope of the current, denoted as $i_{in}(t)$ ($M_c = m_{21} + m_{22}$). This particular value represents the optimal setting for the compensation ramp, intended to mitigate the occurrence of the double cycle phenomenon during the first clock cycle.

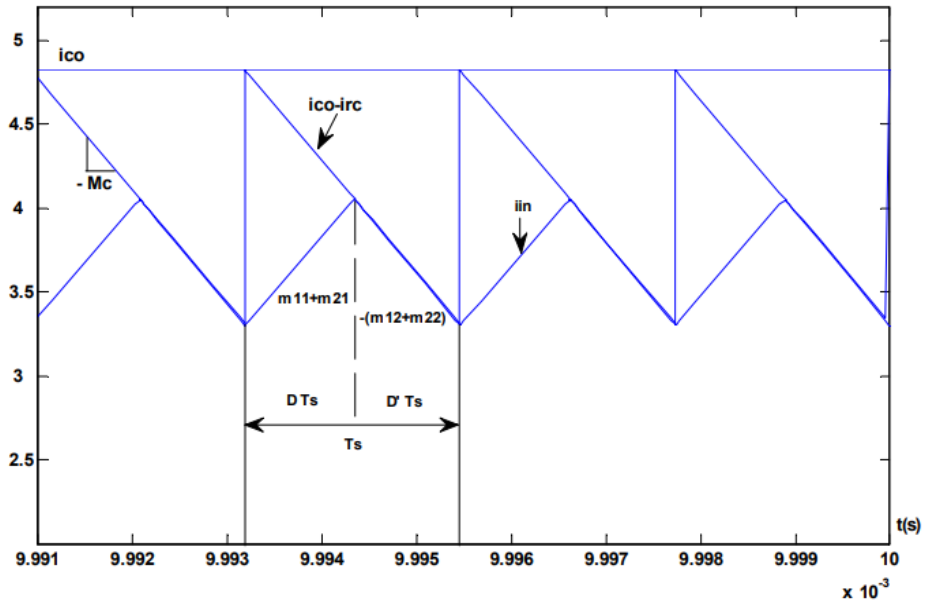

Figure 11. The waveform characteristics of the current at the comparator.

Figures 12 and 13 depict identical signal observations within the Superbuck converter, albeit with peak current mode (PCM) control implemented. A comprehensive performance assessment of the circuit response has been conducted, primarily based on the analysis of current and voltage responses.

The results reveal that the input current, denoted as $i_{in}(t)$, exhibits a pronounced overshoot of 10.2 A. Furthermore, the output current $i_o(t)$, demonstrates an overshoot of 3.2 A, equivalent to 9% of its mean value. Additionally, the output voltage registers an overshoot of 11.2 volts, representing 10% of its average value.

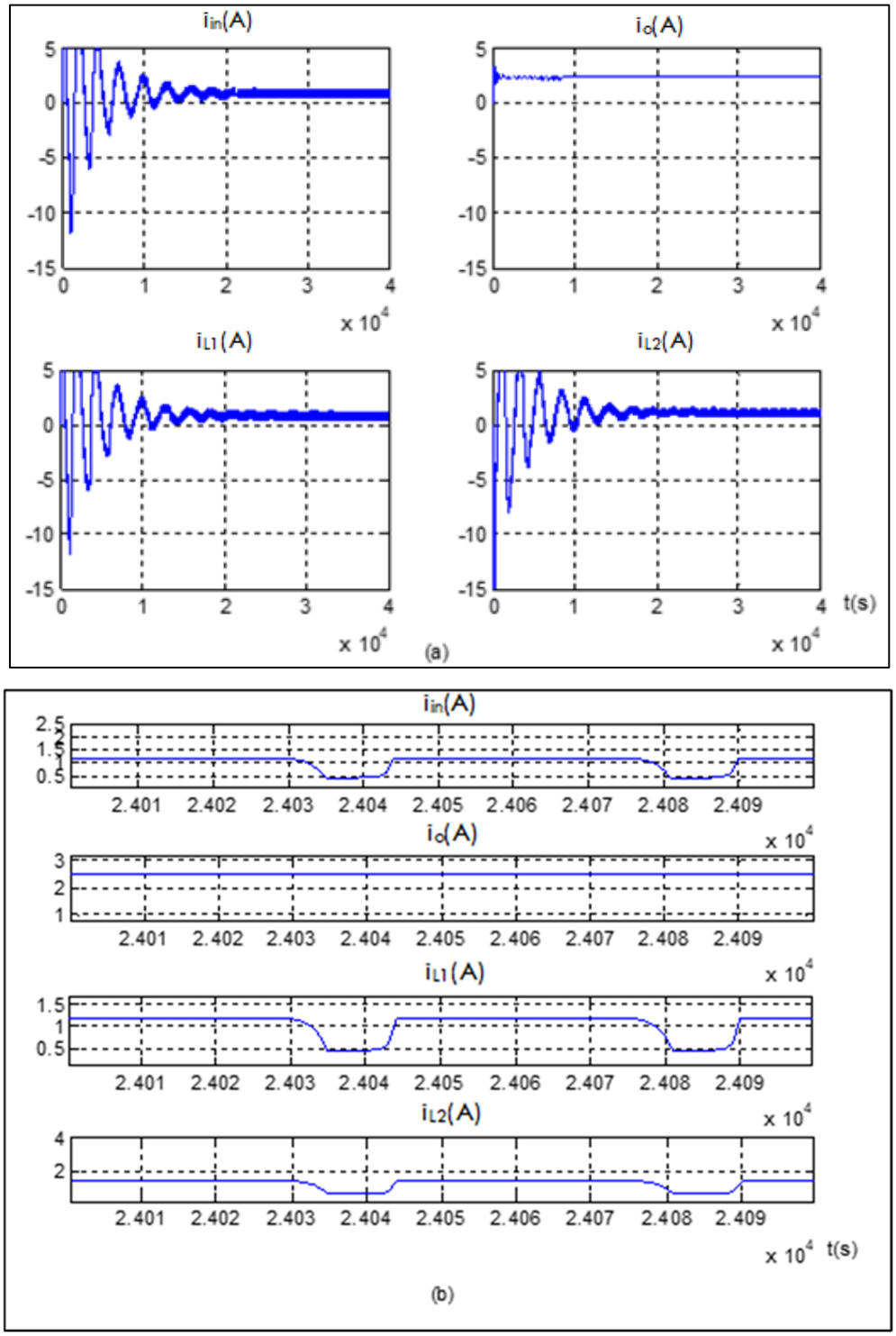

Figure 12. (a) Waveform of the currents $i_{L1}(t)$, $i_{L2}(t)$, $i_{in}(t)$, and $i_o(t)$ of the Superbuck controlled in open loop by the PCM. (b) Waveform of the currents in steady state.

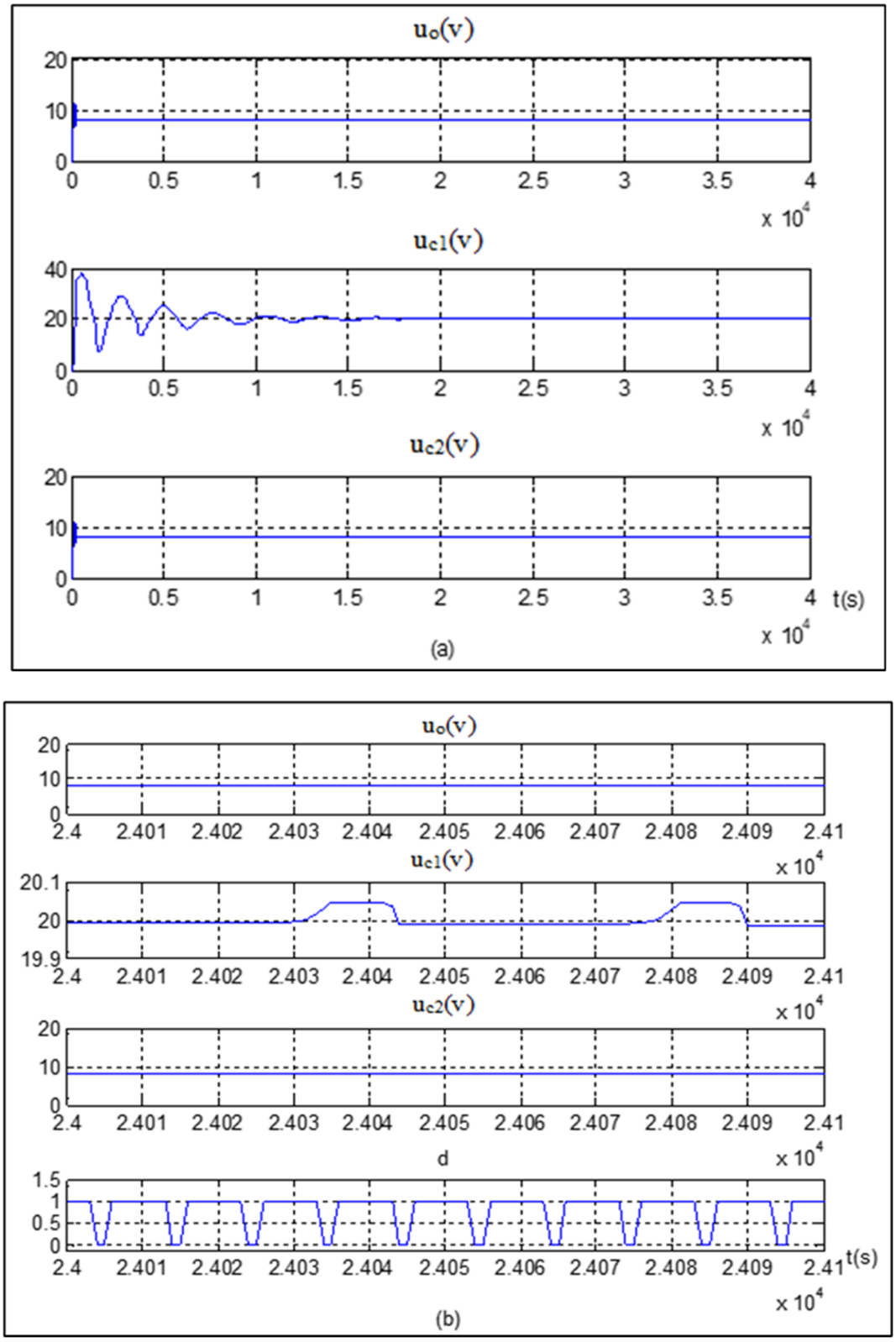

Figure 13. (a) Waveform of the voltages $u_{c1}(t)$, $u_{c2}(t)$, and $u_o(t)$ of the Superbuck controlled in open loop by the PCM. (b) Waveform of the voltages in steady state.

This analysis constitutes fundamental data necessary for initiating a closed-loop study of the system. This involves integrating the controller as defined during the dynamic study to assess whether our system's performance has shown improvement, as referenced in [7,23].

2.2.2. Time-domain analysis of the closed-loop system

The magnitude of ripple in the regulated output current, as well as the voltages $u_{C1}(t), u_{C1}(t)\ and\ u_o(t)$, is notably low. This model's form is presented in Figure 14. Visual representations of the current and voltage waveforms can be found in Figures 15 and 16, respectively. A comprehensive performance analysis of the circuit response is conducted, focusing on the regulated currents and voltages. This analysis reveals that the input current exhibits a noticeable overshoot of 10 amperes. Similarly, the output current experiences an overshoot of 2.6 amperes, constituting approximately 9% of its mean value. Furthermore, the output voltage demonstrates a peak overshoot of 12 volts, which corresponds to 9% of its average value.

Which means that in Figure 15, the sudden variation of the currents i_{in} and io presents a rapid change of charge and causes a disturbance in the system.

For Figure 16, the sudden variation of u_{c1} and u_{c2} induces instability in the regulation loop. So this requires adjusting the PID regulator parameters to keep the output voltage stable and close to the reference value.

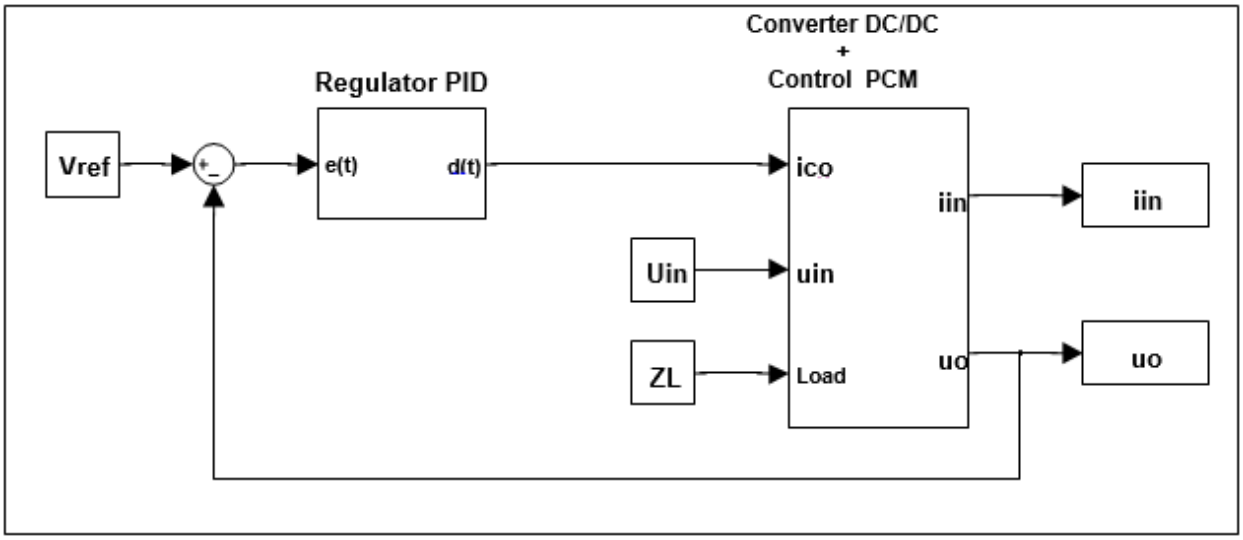

Figure 14. Block diagram depicting the closed-loop control system of the Superbuck converter with PCM-based control.

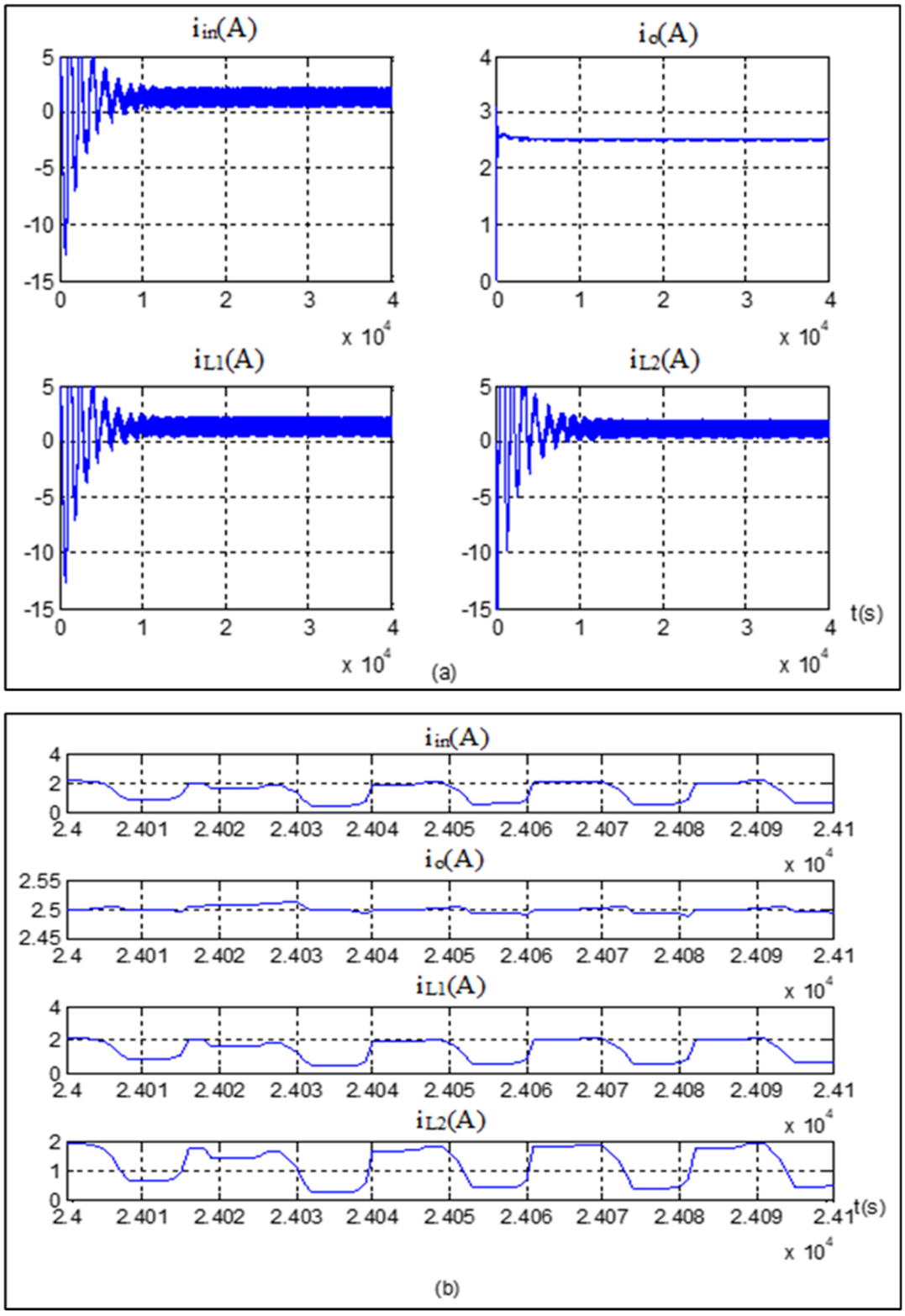

Figure 15. (a) Waveform of the currents $i_{L1}(t)$, $i_{L2}(t)$, $i_{in}(t)$, and $i_o(t)$ of the Superbuck controlled in closed loop by the PCM. (b) Waveform of the currents in steady state.

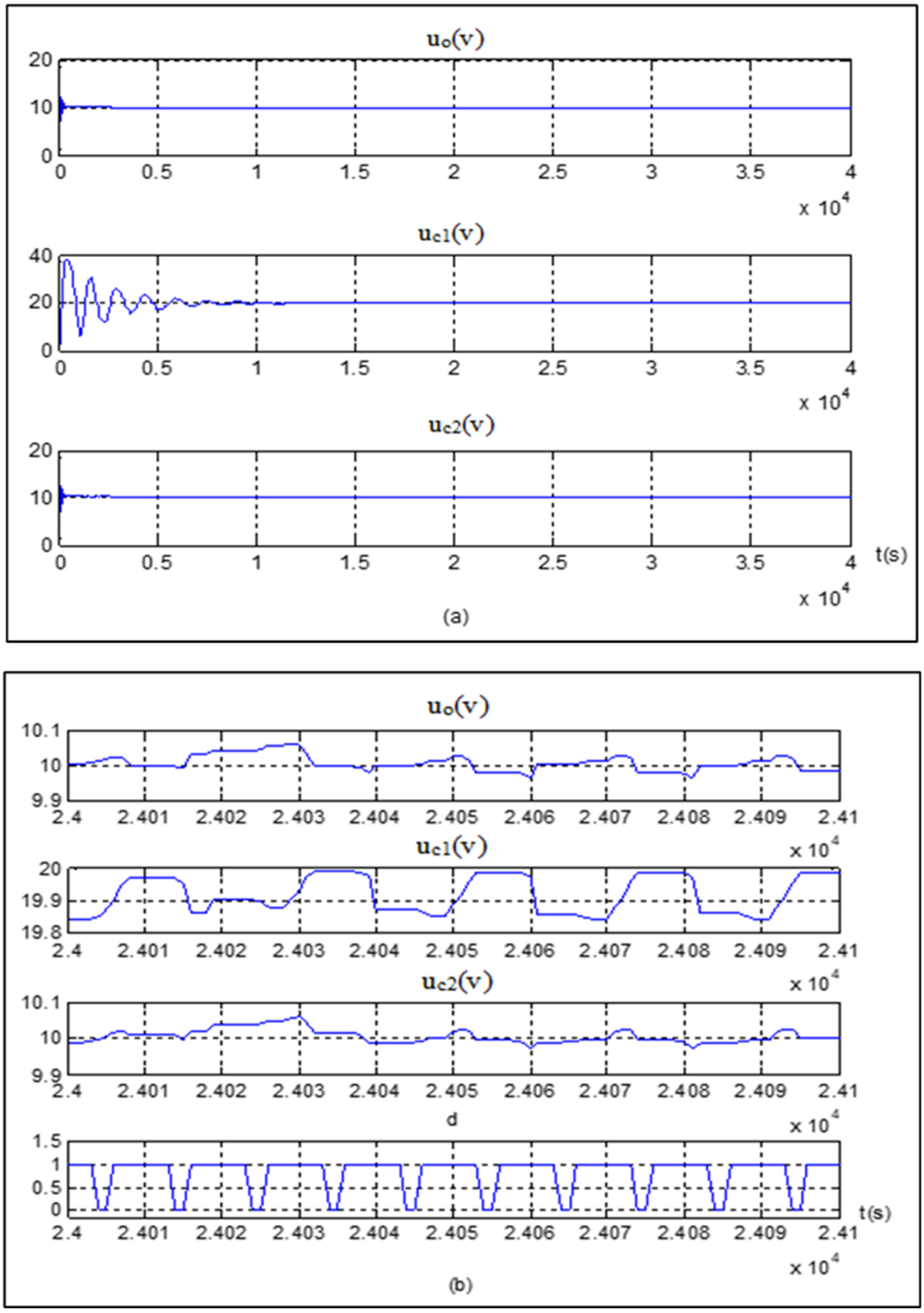

Figure 16. (a) Waveform of the voltages $u_{c1}(t)$, $u_{c2}(t)$, and $u_o(t)$ of the Superbuck controlled in closed loop by the PCM. (b) Waveform of the voltages in steady state.

The impact of the compensation ramp on the converter's performance can be best elucidated through an illustrative example displaying the behavior of the input current. This example is provided in Figure 17.

In the absence of the compensation ramp, resulting in the occurrence of the double cycle phenomenon, the ripple in the input current becomes twice as pronounced compared to when the ramp is incorporated into the current control loop. This disparity is also evident in the input current spectrum, where the presence of a harmonic line is observed in the absence of the ramp, whereas it is absent when the ramp is integrated, as discussed in reference [7].

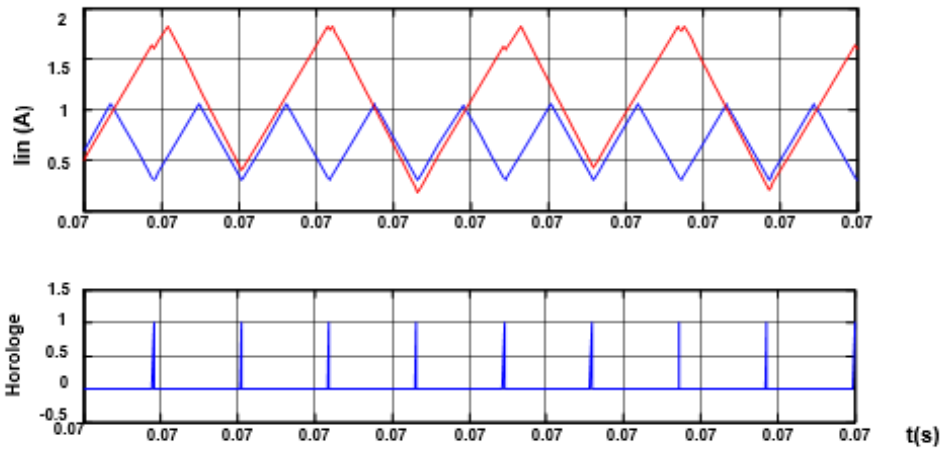

Figure 17. The double cycle phenomenon in the absence of the compensation ramp.

The analysis conducted reaffirms the advantages of this approach, which enables precise current control within the chopper while simultaneously mitigating overshoots in various parameters. Furthermore, it demonstrates the attenuation of resonances observed in the harmonic response of the system. The examination also unveils the phenomenon of double cycling associated with peak current mode (PCM) when the duty cycle (D) exceeds 50%. Additionally, it highlights the influence of the compensation ramp on the system's behavioral characteristics.

3. Experimental results

3.1. Implementation of the PCM control

This section outlines the practical implementation of our work, involving the creation of a prototype comprising a Superbuck converter, which serves as the power board, and a control board built around a Microchip family microcontroller.

The realized converter features components including a MOSFET transistor IRF740, a diode BY30F, two capacitors, and two inductors with specifications provided in Table 1. The selection of the MOSFET transistor as the switching element was based on its ease of control, high efficiency, and rapid switching capabilities. Additionally, a power diode capable of withstanding extreme peak currents in the coil was incorporated. The control technique and control loop were implemented separately to facilitate converter characterization using a Microchip 18F452 microcontroller.

To evaluate the converter's performance, we conducted tests, measuring output voltage, output current, and command pulses for the PCM technique both with and without an electromagnetic filter. Figure 18 illustrates the output voltage, output current, and PCM control pulses at a switching frequency of 100 KHz.

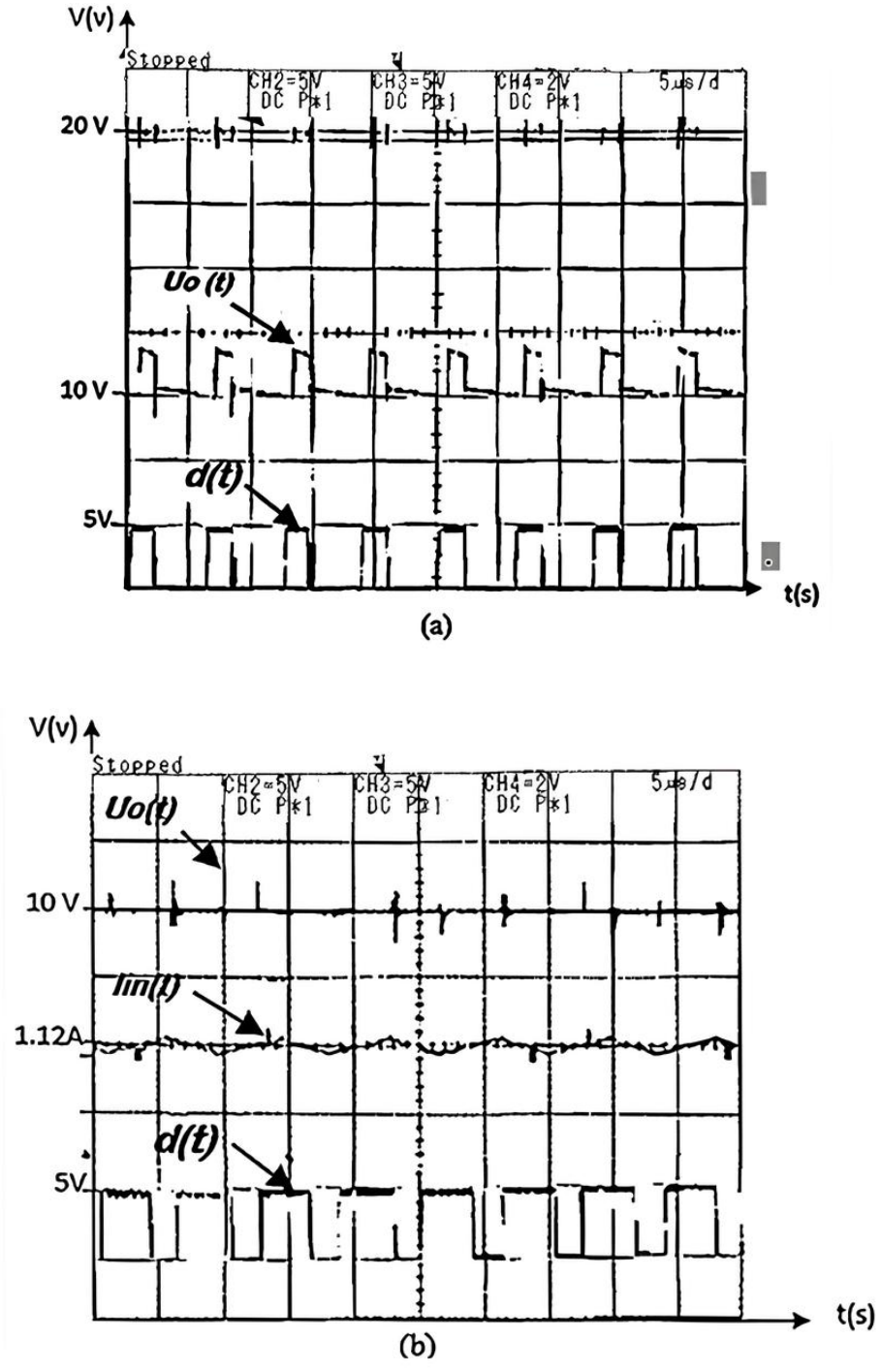

Figure 18. (a) Operation of the Superbuck converter in PCM mode: input voltage, output voltage, control signal (with D = 70%) without the use of an electromagnetic filter. (b) Operation of the Superbuck converter in PCM mode: output voltage, input current, and control signal with the application of an electromagnetic filter.

Figure 19 displays the dual-cycle effect on the input current, attributed to the absence of compensation ramp. Comparative analysis between practical measurements in PCM mode, as presented in Figure 18, and simulation data from Figures 12, 13, 15, and 16 reveals similar results with some tolerance, primarily attributable to delays introduced by the control chain components, such as the driver and the transistor [7].

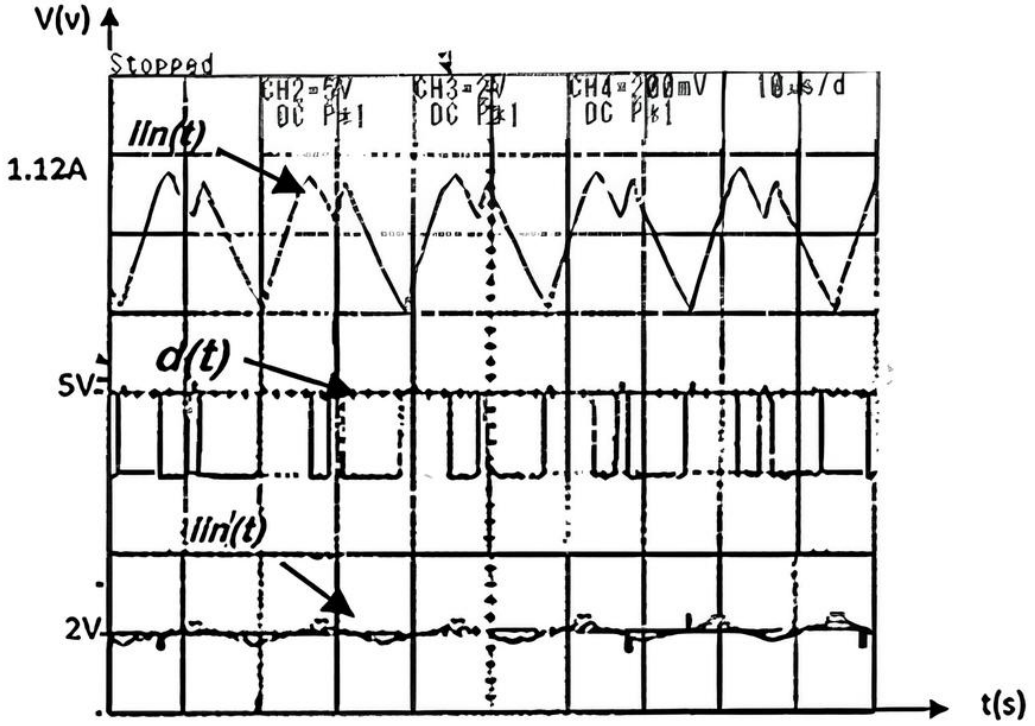

Figure 19. The current $i_{in}(t)$ in the absence of the compensation ramp.

3.2.1. Assessment of the closed-loop converter's performance

Digital control has been adopted for closed-loop operation, with both techniques being implemented within the microcontroller responsible for regulating the output voltage, as depicted in Figure 20.

To assess the stability and performance of our Superbuck converter, a Proportional-Integral-Derivative (PID) controller has been meticulously designed. The task is carried out using the 18F452 microcontroller, which is equipped with essential features, including an analog-to-digital converter, a pulse generator, and, notably, a high clock frequency. To evaluate the efficacy of our controller, two different types of loads, specifically resistive (R) and resistive-inductive-capacitive (RLC), were applied at the output of our converter.

Figures 21 and 22 display the time response of our converter in peak current mode (PCM) mode under resistive and resonant load conditions, respectively. It is apparent that the time response exhibits some delay attributed to the control loop, and the converter demonstrates high output impedance.

Furthermore, it is noteworthy that the output voltage response remains free from oscillations,

signifying the Superbuck converter's load insensitivity.

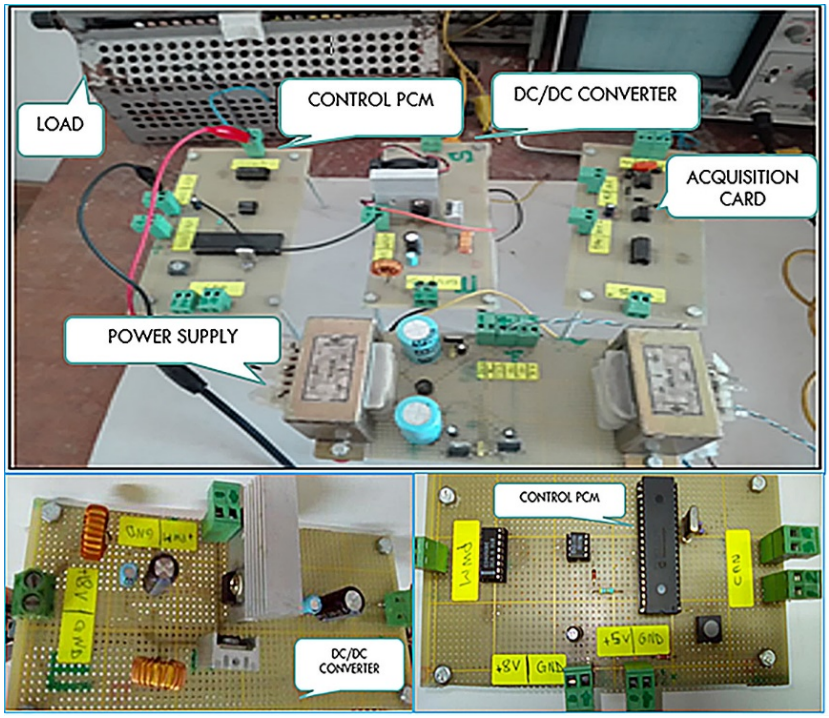

Figure 20. System test bench.

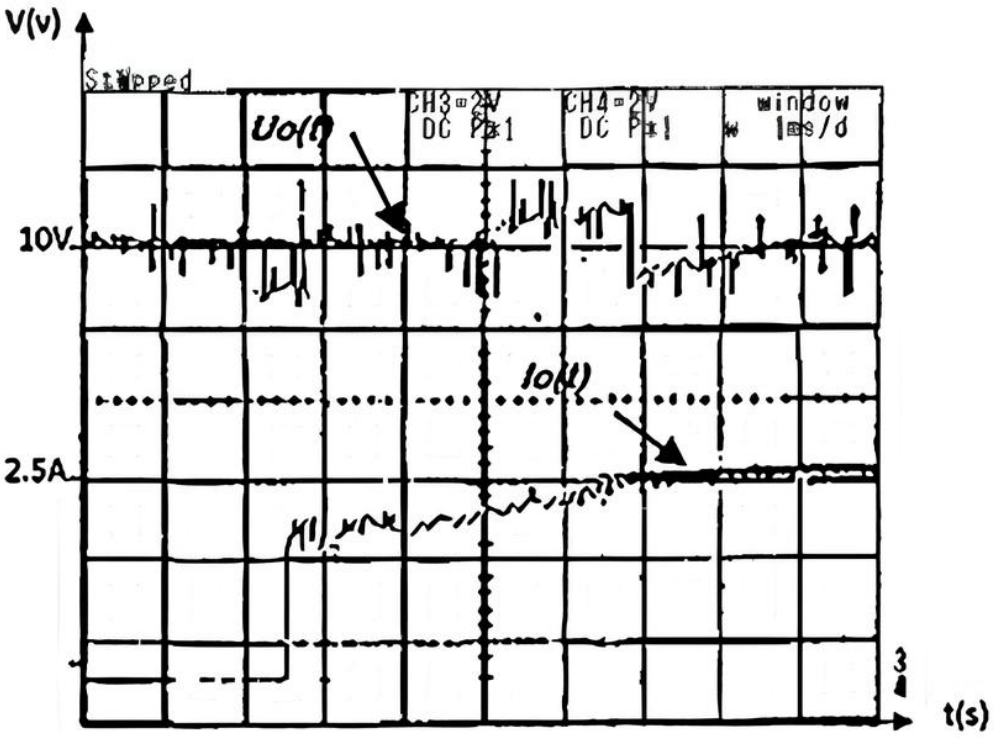

Figure 21. Temporal response of the converter in PCM mode with resistive load.

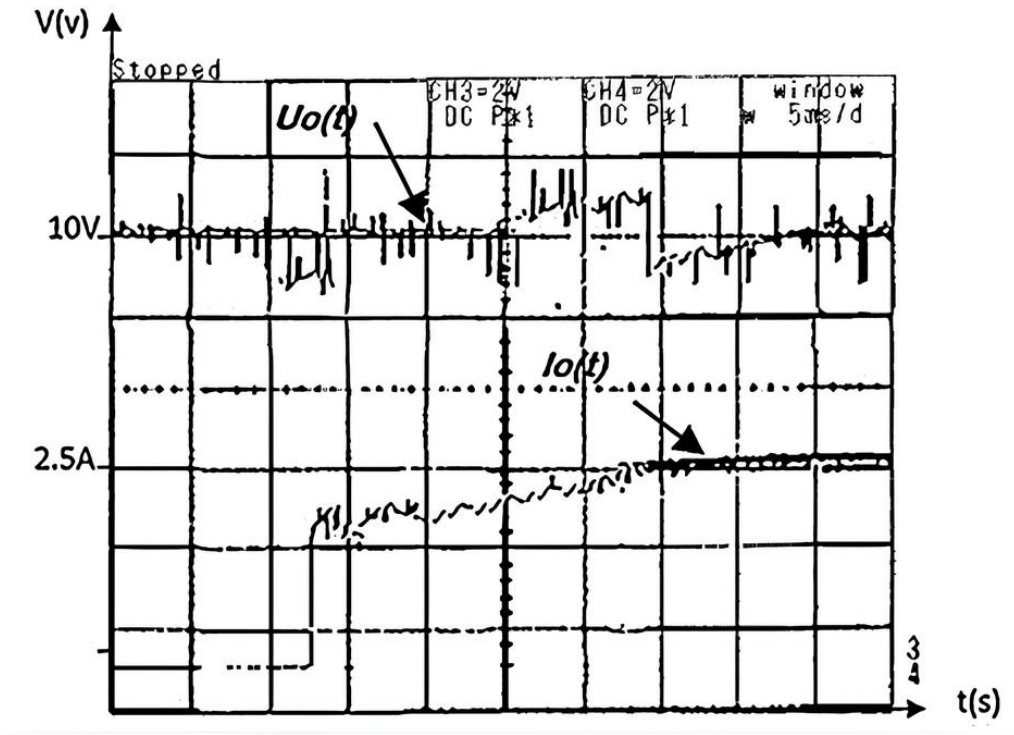

Figure 22. Temporal response of the converter in PCM mode with resonant load.

Empirical measurements confirm the effectiveness of mathematical models in predicting the dynamic behavior of our converter. Specifically, under resistive load conditions, the current mode response exhibits remarkable speed and immediate responsiveness to voltage changes.

Experimental results substantiate a significant improvement in efficiency, with an increase of 4.8% over the base design under a load current of 2.5 A. Additionally, the dynamic response improved compared to the base design.

In simulation, to the VMC control 7 [23], where the overshoots of the different quantities of the circuit have been reduced, the overshoot of the input current, for example, is evaluated at 15 A in VMC 7 [23] when it is 9 A in PCM mode; this makes it possible to obtain a reduction in overrun estimated at 31.24% compared to the VMC. The same observation is made at the level of other quantities, justifying the advantage of PCM in eliminating resonance. Likewise, the establishment times of the quantities are improved compared to the VMC, as well as the response times, except for that of the input current, which has increased by 10% [7].

By comparing the simulation results in Figure 16 with the experimental results in Figure 21 for a resistive load, we distinguish the results mentioned in Table 2. Simulation and experimental results show good agreement, with a maximum percentage error of 1% in the output voltage under a load current of 2.5 A. These small deviations can be attributed to measurement tolerances, which were not fully taken into account in the simulation. Despite this, the overall performance remains consistent, validating the proposed approach.

Table 2. Quantitative analysis of differences between simulation results and experimental results.

Parameter	Simulation result	Experimental result	Percentage error (%)
Output voltage u_o	9.9 V	10 V	1%
Load current i_o	2.55 A	2.5 A	2%
Output ripple ($\Delta \boldsymbol{U}$)	150 mV	100 mV	5%

The measurements carried out practically have proven that the mathematical model gives a good prediction of the dynamic behavior of our converter.

Consequently, PCM is effective in reducing, and in many cases eliminating, the resonance phenomenon that often characterizes the harmonic responses of voltage-mode controlled (VMC) converters. However, it is essential to note that PCM may introduce system instability when the duty cycle (D) exceeds 50%, as indicated in Figure 19 (double cycle phenomenon). This challenge necessitates the application of a compensation ramp to mitigate the phenomenon [7].

To overcome these limitations, it is essential to adapt the characteristics of the inductance and passive components to minimize oscillations and ensure greater stability, particularly for techniques with high duty cycles, such as slope compensation or optimization of converter parameters.

4. Conclusions

For PCM, the analysis conducted has demonstrated the advantage of this method compared to other methods such as VMC (voltage mode control) [7,11], which is the ability to regularly control the current in the chopper while reducing the overshoots of the various parameters and simultaneously verifying the attenuation of the resonances observed in the system's harmonic response. The outcomes highlighted that within the PCM, the introduction of ramping made the converter significantly less susceptible to variations in the source. Nevertheless, it is noteworthy that this control technique exhibited a notable drawback, namely, an elevated output impedance that rendered the Superbuck converter sensitive to fluctuations in load impedance.

Furthermore, we have successfully introduced the PCM into the obtained mathematical model, under which the analysis of the dynamics of the Superbuck converter was possible.

The most significant drawback of PCM manifested when the duty cycle (D) exceeded 50%, necessitating the utilization of a compensation ramp to mitigate instability. Additionally, PCM exhibited limited immunity to noise in the current measurements recorded by the transducer or arising from discrepancies between the output voltage and the reference signal, leading to premature flip-flop resetting and disruptions in circuit operation. Given its sensitivity, substantial fluctuations in the input voltage were intolerable, further compounded by the challenge of controlling low load currents. Ultimately, the practical time study results provided validation for the simulation outcomes, notwithstanding some variations attributed to control-related delays, switching losses, and current spikes stemming from the diode.

AI tools declaration

The authors declare they have not used Artificial Intelligence (AI) tools in the creation of this article.

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Conflict of interest

We declare there is no conflict of interest.

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