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Research article

Power quality enhancement by a solar photovoltaic-based distribution static compensator

Tarun Naruka[1,*], **Debasis Tripathy**[2] **and Prangya Mohanty**[3]

[1] Department of Electrical Engineering, Swami Keshvanand Institute of Technology Management & Gramothan, Ramnagaria, Jaipur, Rajasthan, India
[2] Department of Electrical Engineering, Sandip Institute of Engineering and Management, Nashik, Maharasthra, India
[3] Department of Electrical Engineering, Veer Surendra Sai University of Technology, Burla, Odisha, India

* **Correspondence:** Email: tarun.eic@gmail.com; Tel: +91-7665880996.

Abstract: This work dealt with the design and development of a distributed static compensator (DSTATCOM) for a solar photovoltaic-based grid integrated power system. The DSTATCOM injects or absorbs the reactive power in the power system which maintains the power quality of the power system. The solar photovoltaic-based grid integrated system is comprised of a multi-stage power electronic interface where a quadratic boost converter with a voltage multiplier cell and three-phase DC-AC voltage source inverter are used. The QBC-VMC converter is controlled using variable step size maximum power point tracking. The icosϕ scheme was used for reference current generation as it provides better %THD than the instantaneous reactive power transfer scheme. For DC and AC voltage control, PI controllers were used. Different case studies were considered for the DSTATCOM and respective simulation and experimental analysis was provided. The icosϕ-PI controller control scheme provides lower %THD that is in accordance with the IEEE-519 standard.

Keywords: solar photovoltaic system; DSTATCOM; quadratic boost converter; voltage multiplier cell; icosϕ

1. Introduction

The concept of a microgrid has gained popularity due to its ability to integrate different distributed energy resources (DERs) such as photovoltaic, wind energy, and fuel cell, etc. Among the different DERs, the solar photovoltaic system is one of the most widely used because of the wide availability of solar irradiance and high number of sunny days across the globe. With the abundance of solar

irradiance in a tropical country like India, there is wide acceptance of solar photovoltaic systems and they are installed in household and commercial applications. To encourage the use of DERs, the Government of India has provided different incentives such as a buy-back policy with feed-in-tariffs [1].

The hourly distribution of solar irradiance is modelled using the bimodal Weibull distribution function [2]. The output of the solar photovoltaic system depends on different environmental factors such as solar irradiance, partial shading, and the angle of incident. For integration of DERs to the utility grid, different power electronic converters such as the DC-DC converter and DC-AC inverter are employed [3]. The power electronic converter performs various tasks such as the regulation of active power, voltage and frequency regulation. Adequate control techniques are required for proper operation of the power electronic converter. A state-of-the-art review of various control schemes for the grid-tied inverter has been discussed in [4, 5].

The substantial growth in energy consumptions and use of nonlinear loads such as an uninterrupted power supply, light dimmers, variable frequency drives, etc., burden the power system. To ease the burden on the classical power system, solar power generation is used and most of the solar power generation is carried out on the distribution network nearer to the local communities. The use of nonlinear loads effect the efficiency of the power system and the high switching frequency converters increase the harmonic components in the power system. To reduce the harmonics, passive filters are used that provide fixed compensation but it also has limitation of larger component size and resonance [6]. Therefore, shunt active power filters are used which mitigate the harmonics, providing reactive power compensation as well as power factor correction. There are different methods by which reactive power can be controlled and a state-of-the-art review of these techniques has been highlighted in [7–10]. To curtail the higher losses, different flexible AC transmission systems such as the distributed static compensator (DSTATCOM), dynamic voltage restorer (DVR), and unified power quality conditioner (UPQC), are used in the power system. Solar photovoltaic (SPV) integrated DSTATCOM has been reported in literature that can provide better power quality in the power system. The DSTATCOM is a controlled voltage source converter capable of providing both inductive and capacitive volt-ampere reactive (VAR) (Figure 1).

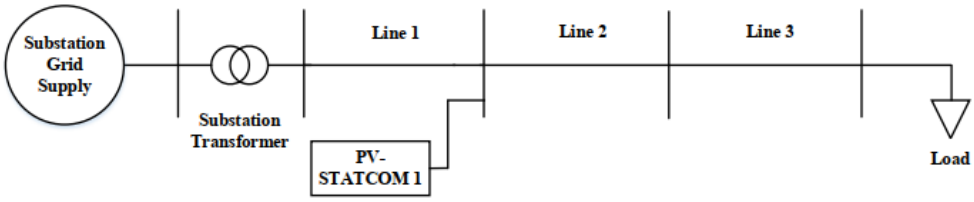


Figure 1. Configuration of DSTATCOM.

The DSTATCOM can act as either a source or sink of reactive power. The DSTATCOM controls the power factor, and detects and compensates for the voltage fluctuations like voltage sag, voltage swell, flickers, etc. (Figure 2). The DSTATCOM provides reactive power compensation in 1 to 2 cycles for very low voltage of 0.2 p.u [11]. The SPV-DSTATCOM is used for stabilizing critical induction motor load [12, 13]. The limits of reactive power in a SPV system are discussed in [14, 15]. The modeling and control aspects of PV-based DSTATCOM are discussed in [16].

There are different types of controllers used for control of the DSTATCOM. There are two different

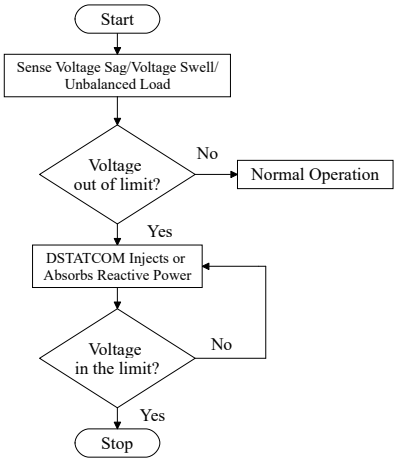


Figure 2. Compensation technique of the DSTATCOM.

Table 1. Summary of different controllers used in the DSTATCOM.

Reference	Control Scheme	Compensation	Controller Complexity
[21]	Adaptive PI Controller	Voltage Sag and Voltage Swell	Low
[22]	Hysteresis Current Controller	Unbalanced Load	Medium
[23]	Model Predictive Controller	Voltage Unbalance	Medium
[24]	Fuzzy Logic Controller	Voltage Sag and Voltage Swell	Medium
[25]	Fractional-Order Sliding Mode Control	Voltage Sag, Voltage Swell and Unbalanced Load	Low

types of control loops in DSTATCOM, i.e., the outer voltage loop that controls the DC link voltage and the inner current loop that generates reference current and the switching signal for the insulated-gate bipolar transistor (IGBT). To generate reference current, instantaneous reactive power theory (IRPT) [17], modified IRPT, and icosϕ [18, 19] techniques are widely used. For DC-link control, different controllers such as the conventional PI controller, model predictive control, etc., are used [20].

For grid integration of SPV systems, a power electronic interface (PEI) is used. The PEI is comprised of a DC-DC converter and DC-AC inverter [26]. For the DC-DC converter, most of the work uses a boost converter. The small-signal model of the PV-fed boost converter operating in CCM and DCM operating mode was discussed in [27–29]. The canonical model of the DC-DC boost converter has been used to develop a small-signal model of a PV-fed boost converter in [30]. Small-signal modeling of a PV-boost converter operating in incremental conductance maximum power point tracking (MPPT) and its validation using controller hardware in a loop was discussed in [31]. But the boost converter has several limitations such as a moderate voltage conversion ratio (VCR), high reverse recovery loss of the diode, non-minimum phase behavior [32], period doubling bifurcation [33] and high voltage stress on the switch and diode. To increase the VCR and decrease the voltage stress on the switch and diode, different non-isolated and isolated topologies of DC-DC converters are used [34]. Among the different non-isolated DC-DC converter topologies, a quadratic boost converter (QBC) is used which is a modified version of the cascaded boost converter [35, 36]. The VCR of the QBC is a quadratic function of the duty cycle of the DC-DC converter, so it provides a higher VCR. The limitation of the QBC is high voltage stress on the switch, and therefore a voltage multiplier cell (VMC) [37] is used along with the QBC. The QBC-VMC converter provides substantially higher VCR than the boost converter and lower voltage stress than the boost converter. In the maximum power point tracking (MPPT) part of the SPV system, most of the papers use the standard perturb and observe P&O

MPPT or incremental conductance MPPT. These MPPTs have a fixed step size and suffer from lower tracking efficiency and drift [38]. Therefore, a modified variable size P&O MPPT is used that can provide an improved tracking efficiency.

This paper provides a detailed analysis of reactive power compensation and harmonic mitigation in a grid-integrated SPV system. In this work a two-stage PEI is used where a QBC-VMC converter and 3-ϕ DC-AC inverter is used. For extraction of maximum power from the SPV, modified variable step size P&O MPPT is used. The DSTATCOM provides reactive power management as well as harmonic mitigation. For control of the DSTATCOM, DC voltage control and AC voltage control are used. The standard PI controllers are used for voltage control. For extraction of reference current, a Icosϕ control scheme is used. Simulation and experimental analysis has been provided which validates the theoretical narrative.

The paper is organized as follows. In Section 2, the system description of the SPV-DSTATCOM is provided which is comprised of a QBC-VMC converter and DSTATCOM. Section 3 provides the control scheme of the SPV-DSTATCOM with the variable step size P&O MPPT scheme, icosϕ algorithm for reference current generation, and PI controller for AC and DC voltage control. Section 4 provides simulation results of the SPV-DSTATCOM with different case studies. Section 5 provides experimental analysis and Section 6 provides concluding remarks for the paper.

2. System description

The complete power circuit and control scheme for the SPV-DSTATCOM is illustrated in Figure 3. The studied system is comprised of SPV panels, a DC-DC converter, and a 3-ϕ voltage source inverter (VSI). The 3-ϕ VSI coupled with filters is connected to the distribution system using a $\Delta - Y$ isolation transformer. The filter components are used to mitigate the harmonics generated by the VSI. To limit the current ripple of the VSI, reactance of the filter inductor is selected between 0.1 to 0.25 pu. The filter capacitor C_f is connected in Δ configuration and it is used to limit the exchange of reactive power below 0.05 pu of the inverter rating. The filter capacitor is connected along with damping resistor R_d.

The characteristics of the SPV are highly nonlinear as evident from the V-I and P-V characteristics. The output of the SPV is dependent on the climatic condition (i.e., solar irradiance, ambient temperature, tilt angle of the solar panel, soiling on the solar panel, snow conditions, etc.). The maximum power of the SPV system is generated at the knee point (MPP) of the P-V characteristics of the solar panel. The MPP keeps on changing with the change in climatic conditions. Therefore, the MPP tracking system is employed to track the changing MPP. To track the change of MPP, power electronic converters are used. The power electronic converter achieves impedance matching and efficiently tracks the MPP [39]. The SPV power is supplied to the DC bus using a DC-DC converter.

2.1. SPV panel

The generalized formula for the single-diode model can be represented as

$$I_{PV} = I_{ph} - I_o\left(e^{\frac{q(V_{PV}+R_sI_{PV})}{AKT_{STC}}} - 1\right) - \frac{V_{PV} + R_sI_{PV}}{R_p} \tag{2.1}$$

In Eq 2.1, there are five independent parameters, i.e., photo current I_{PV}, saturation current I_o, thermal voltage timing completion factor a, R_s, and R_p.

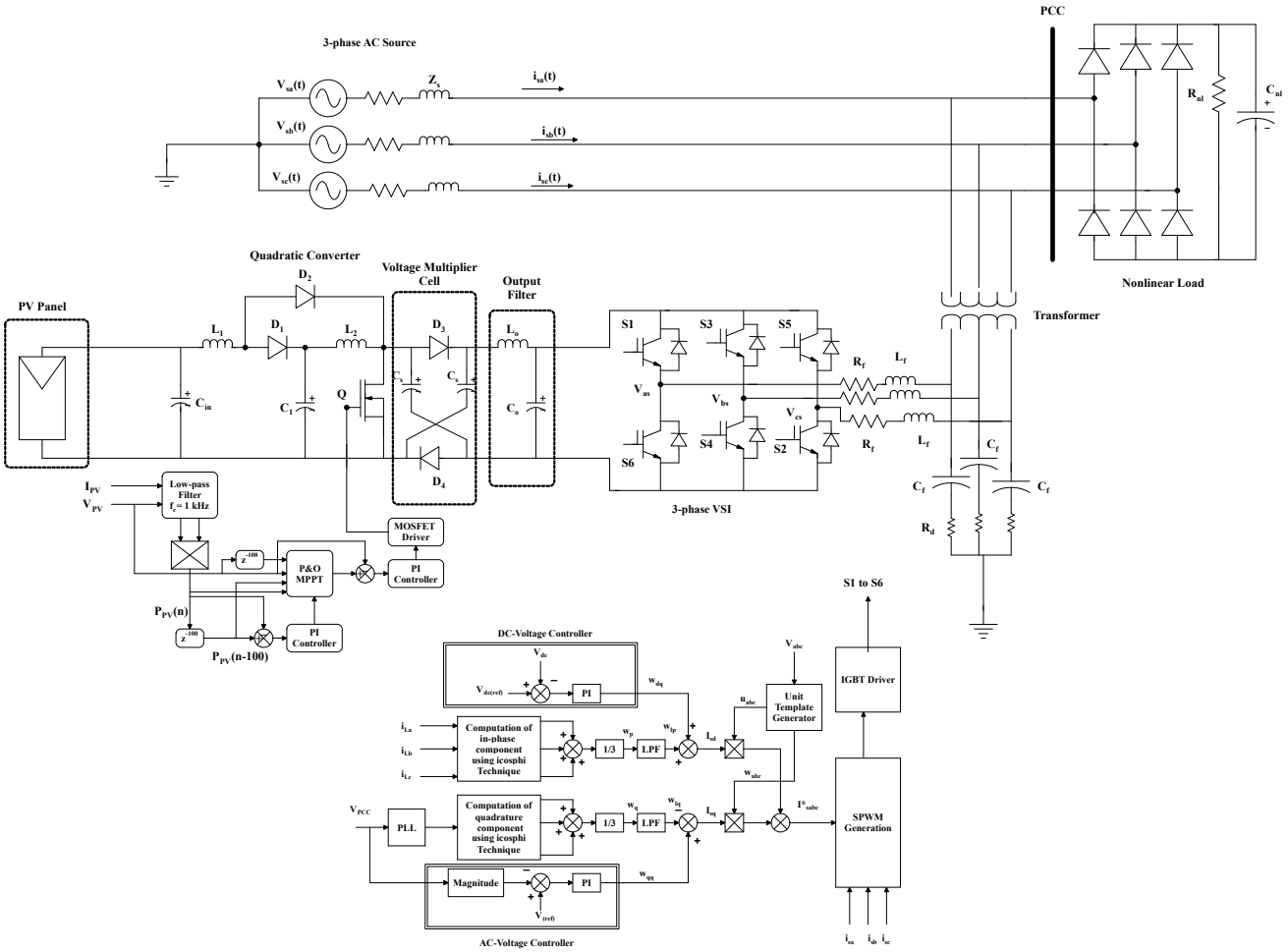


Figure 3. Power circuit and control scheme of the PV-DSTATCOM.

For the analytical solution of this parameter extraction problem, Eq 2.1 is written at three key points, i.e., open circuit voltage V_{OC}, short circuit current I_{sc}, and maximum power point V_{mp} and I_{mp}.

At $I_{pv} = 0$ and $V_{pv} = V_{oc}$,

$$0 = I_{ph} - I_o\left(e^{\frac{q(V_{OC})}{AKT_{STC}}} - 1\right) - \frac{V_{OC}}{R_p} \tag{2.2}$$

At $I_{pv} = I_{sc}$ and $V_{pv} = 0$,

$$I_{sc} = I_{ph} - I_o\left(e^{\frac{q(V_{OC})}{AKT_{STC}}} - 1\right) - \frac{R_s I_{sc}}{R_p} \tag{2.3}$$

At $I_{pv} = I_{mp}$ and $V_{pv} = V_{mp}$,

$$I_{mp} = I_{ph} - I_o\left(e^{\frac{q(V_{mp}+R_s I_{mp})}{AKT_{STC}}} - 1\right) - \frac{V_{mp} + R_s I_{mp}}{R_p} \tag{2.4}$$

The series and shunt resistance can be defined as

$$R_s = -\left.\frac{dI_{PV}}{dV_{PV}}\right|_{V_{PV}=V_{OC}} \tag{2.5}$$

$$R_p = -\left.\frac{dI_{PV}}{dV_{PV}}\right|_{I_{PV}=I_{SC}} \tag{2.6}$$

The diode modified quality factor at STC is

$$a_{STC} = \frac{V_{mp} + R_{so}I_{mp} - V_{OC}}{\ln\left(I_{sc} - \frac{V_{mp}}{R_{sho}} - I_{mp}\right) - \ln\left(I_{sc} - \frac{V_{oc}}{R_o}\right) + \frac{I_{mp}}{I_{sc} - \frac{V_{oc}}{R_{so}}}} \tag{2.7}$$

The reverse leakage current at STC is

$$I_{0STC} = \left(I_{sc} - \frac{V_{OC}}{R_p}\right) e^{\left(-\frac{V_{OC}}{a}\right)} \tag{2.8}$$

The photocurrent at STC is

$$I_{phSTC} = I_{sc}\left(1 + \frac{R_s}{R_p}\right) + I_o e^{\left(\frac{I_{sc}R_s}{a} - 1\right)} \tag{2.9}$$

2.2. QBC-VMC converter

The resistance seen by the solar module is

$$R_{in} = f(d)\, R_o \tag{2.10}$$

where R_{in} is the input resistance of the converter, and R_o is the output resistance of the converter. The function of duty cycle that depends on the converter selection is $f(d) \in \{0, 1\}$.

There are different types of DC-DC converter topologies available in the literature and the topologies can be broadly classified as non-isolated DC-DC converter topology and isolated DC-DC converter topology. Among non-isolated converter topology, most of the power electronic design engineer uses a step-up DC-DC boost-type converter.

The load inclination angle of the PV-fed boost converter feeding a resistive load is

$$\theta = \tan^{-1}\left(\frac{1}{(1-d)^2 R}\right) \tag{2.11}$$

When $d = 0$, the minimum load inclination angle is $\theta = \tan^{-1}\left(\frac{1}{R}\right)$ and when $d = 1$, the maximum load inclination angle is 90°.

The temperature range that ensures the system is operating on the tracking region is defined as

$$T \geq T^{STC} - \frac{V_{DC} - V_{mp}^{STC}}{\left|\mu_{Vmp}\right|} \tag{2.12}$$

where μ_{Vmp} is the temperature voltage co-efficient.

But the boost-type converter has different limitations such as a lower voltage conversion ratio (VCR), higher reverse recovery losses of the power diode, and non-minimum phase behavior of the transfer function of the boost converter. To mitigate the limitations of the boost converter, a quadratic boost converter (QBC) is employed. In a QBC, the VCR is the quadratic function of the duty cycle.

Though the QBC improves the VCR, the voltage stress on the switch of the QBC is very high. To reduce the voltage stress on the switch of the QBC, a diode-capacitor voltage multiplier cell (VMC) is used.

The comparison of different DC-DC converters is shown in Table 2. The QBC-VMC converter (Figure 4) is comprised of 4 diodes D_1 to D_4, 3 inductors L_o to L_2, and 4 capacitors. The input capacitor with the SPV system is used to mitigate any ripple in the SPV voltage. The switch is controlled using a PWM signal computed from variable step size MPPT. The detailed analysis of the QBC-VMC converter integrated with a SPV panel can be found in [40].

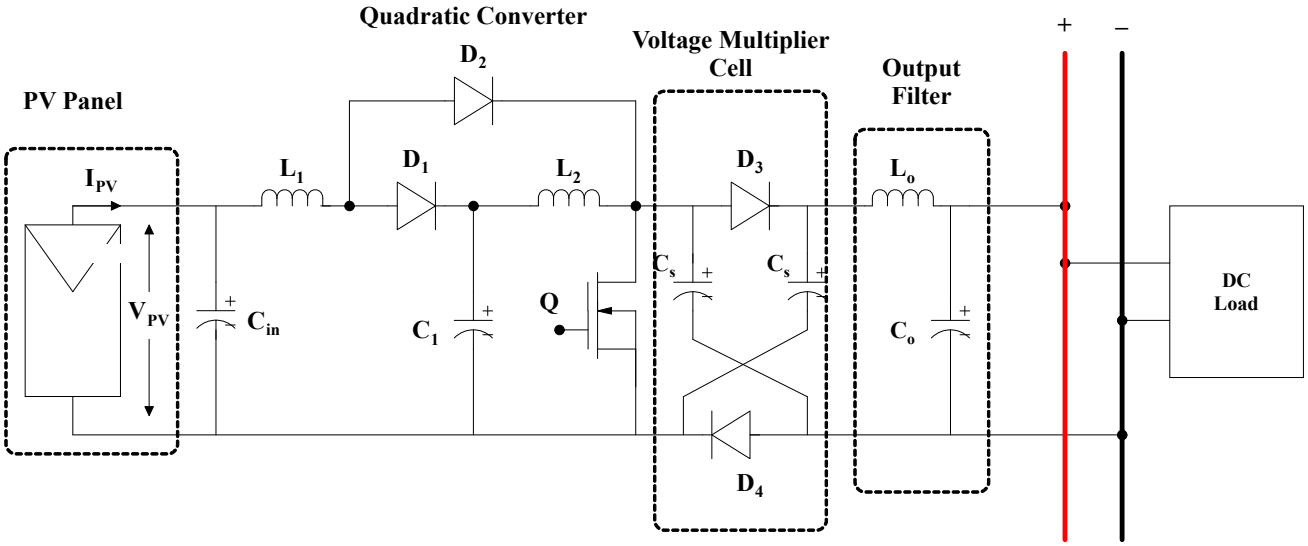


Figure 4. Circuit diagram of the QBC-VMC converter.

Table 2. Comparative analysis of different DC-DC converters.

	Boost Converter	QBC	QBC-VMC (This work)
Switches	1	1	1
Diodes	1	3	4
Inductors	1	2	3
Capacitors	1	2	4
VCR	$\frac{1}{1-d}$	$\frac{1}{(1-d)^2}$	$\frac{1+d}{(1-d)^2}$
Voltage stress of switch	V_{DC}	V_{DC}	$\frac{V_{DC}}{1+d}$
Voltage stress across diode	V_{DC}	V_{DC}	$\frac{(1-d)V_{DC}}{1+d}$

2.3. DSTATCOM

Using the Kirchoff Voltage Law at point of common coupling (PCC), we get

$$\begin{aligned} V_{as} &= i_{as}R_f + L_f\frac{di_{as}}{dt} + V_{sa} \\ V_{bs} &= i_{bs}R_f + L_f\frac{di_{bs}}{dt} + V_{sb} \\ V_{cs} &= i_{cs}R_f + L_f\frac{di_{cs}}{dt} + V_{sc} \end{aligned} \tag{2.13}$$

Equation 2.13 can be written in matrix form as

$$\frac{d}{dt}\begin{bmatrix} i_{as} \\ i_{bs} \\ i_{cs} \end{bmatrix} = \begin{bmatrix} -\frac{R_f}{L_f} & 0 & 0 \\ 0 & -\frac{R_f}{L_f} & 0 \\ 0 & 0 & -\frac{R_f}{L_f} \end{bmatrix}\begin{bmatrix} i_{as} \\ i_{bs} \\ i_{cs} \end{bmatrix} + \frac{1}{L_s}\begin{bmatrix} V_{as} - V_{sa} \\ V_{bs} - V_{sb} \\ V_{cs} - V_{sc} \end{bmatrix} \tag{2.14}$$

Using Park's transformation, we get

$$\begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} = \frac{2}{3}\begin{bmatrix} \cos\theta & \cos\left(\theta - \frac{2\pi}{3}\right) & \cos\left(\theta + \frac{2\pi}{3}\right) \\ -\sin\theta & -\sin\left(\theta - \frac{2\pi}{3}\right) & -\sin\left(\theta + \frac{2\pi}{3}\right) \\ 0.5 & 0.5 & 0.5 \end{bmatrix}\begin{bmatrix} i_{as} \\ i_{bs} \\ i_{cs} \end{bmatrix} \tag{2.15}$$

Equation 2.15 can be written as

$$\frac{d}{dt}\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} -\frac{R_f}{L_f} & \omega \\ \omega & -\frac{R_f}{L_f} \end{bmatrix}\begin{bmatrix} i_d \\ i_q \end{bmatrix} + \frac{1}{L_f}\begin{bmatrix} e_d - v_d \\ v_q - e_q \end{bmatrix} \tag{2.16}$$

$$\frac{d}{dt}\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} -\frac{R_f}{L_f} & \omega \\ \omega & -\frac{R_f}{L_f} \end{bmatrix}\begin{bmatrix} i_d \\ i_q \end{bmatrix} + \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} \tag{2.17}$$

In Eq 2.17,

$$\begin{aligned} x_1 &= \tfrac{1}{L_f}(e_d - v_d) \\ x_2 &= -\tfrac{1}{L_f} e_q \end{aligned} \tag{2.18}$$

where

$$\begin{aligned} e_d &= kV_{dc}\cos\alpha \\ e_q &= kV_{dc}\sin\alpha \end{aligned} \tag{2.19}$$

3. Control scheme for the SPV-DSTATCOM

The complete SPV-DSTATCOM control scheme is comprised of the following controller and auxiliary blocks:

- MPPT Unit: For tracking of MPPT in SPV panel and impedance matching with DC-DC converter
- AC Controller
- Phase Locked Loop
- DC Controller

3.1. Variable step size P&O MPPT

An MPPT system is used to provide impedance matching to the SPV panel in varying environmental parameters. The traditional perturb and observe MPPT has fixed perturbation size that has large oscillations in a steady-state condition. Therefore, variable step size MPPT is used (Figure 5). In variable step size MPPT, the current and voltage of the SPV panel V_{PV} and I_{PV} are measured and passed through a low pass filter of cut off frequency 1 kHz. The power of the SPV panel is determined by multiplying V_{PV} and I_{PV}. The P&O MPPT and two PI controllers are used in variable step size MPPT and the output of MPPT is provided to the PWM unit to generate switching signals to the QBC-VMC converter.

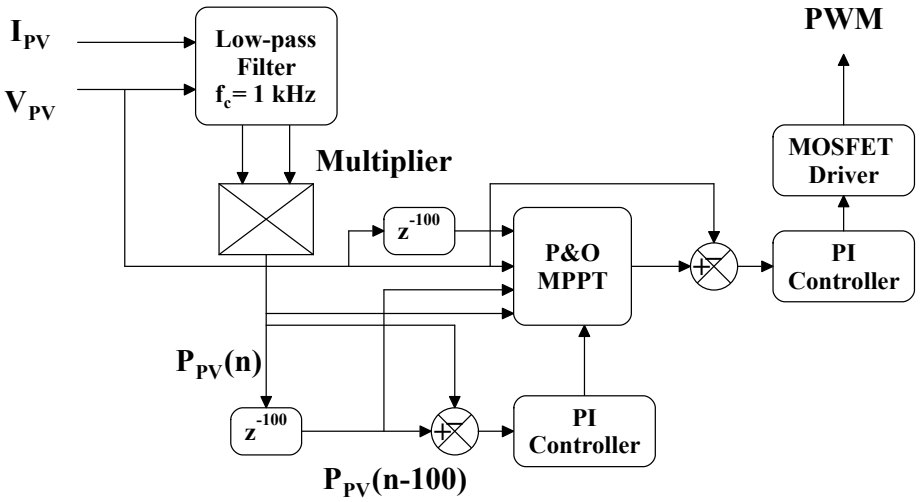


Figure 5. Variable step size MPPT.

3.2. PLL

The PLL is comprised of a feedback loop based on a synchronous rotating frame (SRF-PLL) can precisely extract a voltage synchronization signal from 3-ϕ grid voltage that is symmetrical and without any distortion. The SRF-PLL is used in stiff-grid conditions. Consider a balanced 3-ϕ utility grid voltage,

$$v_{abc} = V_m \begin{pmatrix} \cos\theta \\ \cos\left(\theta - \frac{2\pi}{3}\right) \\ \cos\left(\theta + \frac{2\pi}{3}\right) \end{pmatrix} \tag{3.1}$$

Using the Clarke transform, the utility voltage can be transformed into SRF:

$$v_{\alpha\beta} = \frac{2}{3} \begin{pmatrix} 1 & -0.5 & -0.5 \\ 0 & -\frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{pmatrix} v_{abc} \tag{3.2}$$

The d-q transformation is represented as

$$v_{qd} = \begin{pmatrix} \cos\hat{\theta} & -\sin\hat{\theta} \\ \sin\hat{\theta} & \cos\hat{\theta} \end{pmatrix} v_{\alpha\beta} \tag{3.3}$$

The direct component voltage can be represented as

$$v_d = V_m \sin\left(\hat{\theta} - \theta\right) = E_m \sin\delta \tag{3.4}$$

The angular frequency of PLL can be represented as

$$\hat{\omega} = \frac{d\hat{\theta}}{dt} = K_f e \tag{3.5}$$

where K_f is the loop gain of the transfer function.

The frequency and phase angle of the PLL is used to track the frequency and phase angle of the utility grid.

3.3. icosϕ-based reference current extraction

The control scheme of the DSTATCOM is illustrated in Figure 6 where the load currents i_{La}, i_{Lb}, and i_{Lc} are measured and these currents have a lot of harmonics as represented in Eq 3.6. The load currents are decomposed into three different components such as the fundamental direct component, fundamental quadrature component, and harmonic component as represented in Eq 3.7. To extract the fundamental component of the load current, the load current is passed through a second-order low pass filter (the cut-off frequency f_c of LPF is 50 Hz).

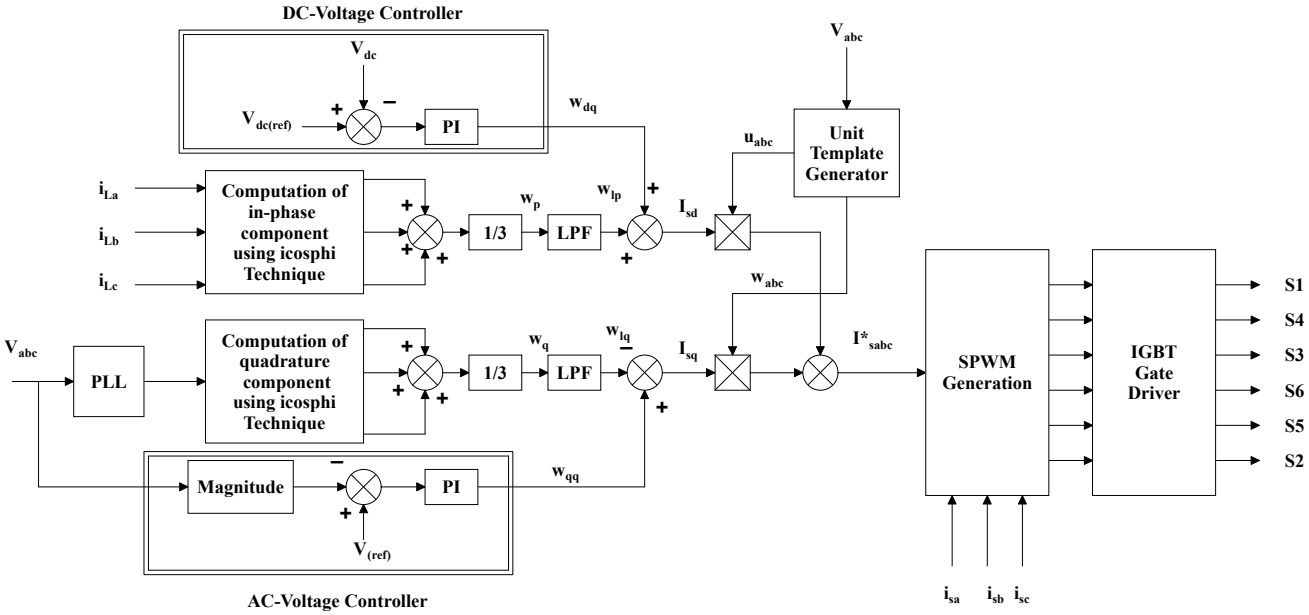


Figure 6. Control scheme of DSTATCOM.

$$\begin{aligned} i_{La} &= i_{Lfa}\sin(\omega t-\theta_a)+\sum_{n=2}^{\infty} I_{Lna}\sin(n\omega t-\theta_{na}) \\ i_{Lb} &= i_{Lfb}\sin(\omega t-\theta_b)+\sum_{n=2}^{\infty} I_{Lnb}\sin(n\omega t-\theta_{nb}) \\ i_{Lc} &= i_{Lfc}\sin(\omega t-\theta_c)+\sum_{n=2}^{\infty} I_{Lnc}\sin(n\omega t-\theta_{nc}) \end{aligned} \tag{3.6}$$

$$\begin{aligned} i_{La} &= I_{Lfa}\cos\theta_a + I_{Lfa}\sin\theta_a + \text{HarmonicComponent} \\ i_{Lb} &= I_{Lfb}\cos\theta_b + I_{Lfb}\sin\theta_b + \text{HarmonicComponent} \\ i_{Lc} &= I_{Lfc}\cos\theta_c + I_{Lfc}\sin\theta_c + \text{HarmonicComponent} \end{aligned} \tag{3.7}$$

For DC-link voltage regulation, a proportional-integral (PI) controller is used and similarly, the voltage oscillation in PCC is regulated using the PI controller which can be represented as

$$G_c^{PI}(s) = \frac{K_p s + K_i}{s(1+\lambda s)} \tag{3.8}$$

where K_p is the proportional gain and K_i is the integral gain of the PI controller and λ is the filter coefficient.

A frequency response-based method is used to find the gain and phase margin of the system and using the gain and phase margin, the values of K_p and K_i can be found out.

The direct unit vector component of 3-ϕ balanced supply voltage can be expressed as Eq 3.9:

$$\begin{bmatrix} u_{da} \\ u_{db} \\ u_{dc} \end{bmatrix} = \frac{1}{\sqrt{\frac{2}{3}\left(v_{sa}^2 + v_{sb}^2 + v_{sc}^2\right)}} \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} v_{sa} \\ v_{sb} \\ v_{sc} \end{bmatrix} \tag{3.9}$$

The quadrature unit vector component of 3-ϕ balanced supply voltage can be expressed as Eq 3.10:

$$\begin{bmatrix} u_{qa} \\ u_{qb} \\ u_{qc} \end{bmatrix} = \frac{1}{2\sqrt{3}} \begin{bmatrix} 0 & -2 & 2 \\ 3 & 1 & -1 \\ -3 & 1 & -1 \end{bmatrix} \begin{bmatrix} u_{da} \\ u_{db} \\ u_{dc} \end{bmatrix} \tag{3.10}$$

Reference source current is used to obtain the desired switching pulses for the DSTATCOM. The direct component of the reference source current is expressed as

$$\begin{bmatrix} i_{sad}^* \\ i_{sbd}^* \\ i_{scd}^* \end{bmatrix} = I_{sd} \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} u_{da} \\ u_{db} \\ u_{dc} \end{bmatrix} \tag{3.11}$$

The quadrature component of the reference source current is computed as

$$\begin{bmatrix} i_{saq}^* \\ i_{sbq}^* \\ i_{scq}^* \end{bmatrix} = I_{sq} \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} u_{qa} \\ u_{qb} \\ u_{qc} \end{bmatrix} \tag{3.12}$$

The current error can be computed by subtracting the sensed source current from the reference source current and the current error is processed through a hysteresis current control scheme to generate the desired switching pulses. For pulse width modulation (PWM) generation, sinusoidal PWM is used. The generated switching pulses are provided to the 2-level IGBT-based VSI using an appropriate gate driver and isolation circuit.

4. Simulation results

For simulation of the SPV-fed DSTATCOM and validation of its control schemes using MATLAB-Simulink, the simulation parameters in Table 3 are considered.

4.1. Performance evaluation of the MPPT

The DC-link voltage at a standard test condition (STC) (solar irradiance of 1000 W/m^2 and temperature of 25°C) is shown in Figure 7(a) where the reference DC link voltage is tracked by the MPPT scheme. During the ramp increase in solar irradiance, the reference DC-link voltage is maintained by the MPPT scheme (Figure 7(b)). The DC-link voltage with non-uniform solar irradiance is shown in Figure 7(c) where there is a sharp decrease of solar irradiance at 1 min and a sharp increase of the solar irradiance. The resultant PV voltage and PV current are shown. The DC-link voltage is maintained by the MPPT scheme.

Algorithm 1: Design procedure for QBC-VMC converter.

Step 1: Measure the SPV module voltage and current V_{PV}, I_{PV} and compute power P_{PV}

Step 2: The DC-link voltage is

$$V_{DC} = \frac{2\sqrt{2}V_{LL}}{\sqrt{3}m} \tag{4.1}$$

In Eq. 4.1, m denotes the modulation index of VSI

Step 3: Due to any voltage surge, energy absorbed by the DC-link capacitor is

$$\Delta P_{dc}\Delta t = \frac{1}{2}C_{dc}(V_{DC} + \Delta V_{DC})^2 - \frac{1}{2}C_{dc}V_{DC}^2 \tag{4.2}$$

In Eq. 4.2, ΔP_{dc} is the change in power, Δt is the time of the voltage surge, and the magnitude of fluctuation of the DC-link is

$$\Delta V_{DC} = \frac{\Delta P_{dc}\Delta t}{C_{dc}V_{DC}} \tag{4.3}$$

Step 4: The design parameters of the QBC-VMC converter are the input voltage V_{PV}, output voltage V_{DC}, and switching frequency f_{sw}. Compute d

Step 5: The maximum allowable current ripple in L_1, L_2, and L_o, is Δi_{L_1}, Δi_{L_2}, and Δi_{L_o} respectively

$$\Delta i_{L_1} = \frac{V_{PV}d}{f_{sw}L_1} \tag{4.4}$$

$$\Delta i_{L_2} = \frac{V_{PV}d}{f_{sw}L_2(1-d)} \tag{4.5}$$

$$\Delta i_{L_o} = \frac{V_{PV}(1+d)}{R(1-d)^2} \tag{4.6}$$

Step 6: The maximum allowable voltage ripple for each capacitor is:

$$\Delta v_{c_1} = \frac{V_{PV}d(1+d)^2}{RC_1f_{sw}(1-d)^3} \tag{4.7}$$

$$\Delta v_{c_s} = \frac{V_{PV}d(1+d)}{RC_sf_{sw}(1-d)^2} \tag{4.8}$$

$$\Delta v_{c_o} = \frac{V_{PV}d}{8L_oC_of_{sw}^2(1-d)} \tag{4.9}$$

Step 7: For continuous conduction mode (CCM) operation of the QBC-VMC converter, the inductors need to satisfy the following limits:

$$L_1 = \frac{Rd(1-d)^4}{2f_{sw}(1+d)^2} \tag{4.10}$$

$$L_2 = \frac{Rd(1-d)^2}{2f_{sw}(1+d)^2} \tag{4.11}$$

$$L_o = \frac{Rd(1-d)}{2f_{sw}(1+d)} \tag{4.12}$$

Step 8: The input capacitor of QBC-VMC C_{in} is designed to filter out the current ripples produced by L_1. The maximum allowable voltage ripple for the input capacitor is denoted as V_{mp}, the maximum duty cycle of the converter is d_{max}:

$$C_{in} = \frac{d_{\max}}{8L_1f_{sw}^2\Delta V_{mp}} \tag{4.13}$$

Step 9: Calculation of the minimum value of the output capacitor:

$$C_o = \frac{I_od}{\Delta V_{c_o}f_{sw}} \tag{4.14}$$

Step 10: The DC-link capacitor for power balance between the converter and inverter is calculated as

$$C_{dc} = \frac{0.9I_{peak}}{4\sqrt{2}\pi f\Delta V_{DC}} \tag{4.15}$$

In Eq.4.15, I_{peak} is the maximum peak AC current, and f is the grid frequency.

Table 3. Simulation parameters.

SPV	Power at STC	P_{STC}	305 W
	Voltage at MPP	V_{mp}	54.7 V
	Current at MPP	I_{mp}	5.58 A
	Short Circuit Current	I_{sc}	5.98 A
	Open Circuit Voltage	V_{oc}	64.2 V
SPV Array	Number of series connected modules	N_s	5
	Number of parallel connected modules	N_p	66
QBC-VMC Converter	Input Capacitor	C_{in}	100μF
	Inductor	L	60μH, 260μH, 750μH
	Capacitor	C	15 μF, 4.7 μF, 0.33 μF
	Switching Frequency	f_{sw}	20 kHz
VSI (DSTATCOM)	Switching Frequency	f_{sw}	20 kHz
Passive Filter	Filter Inductance	L_f	3 mH
Grid Voltage			440 V
Grid Impedance			$R_s = 0.1\Omega$, $L_s = 0.1$ mH

4.2. Case I: Performance of the DSTATCOM with ideal supply voltage and nonlinear load

In Figure 8, the ideal supply voltage and its respective source current at nonlinear load is provided. The total harmonic distortion of the source current is found to be 30.92% (Figure 9). The THD is very high before compensation, therefore, the icosϕ controller is used for compensation. The simulation results of the source current after compensation are shown in Figure 10.

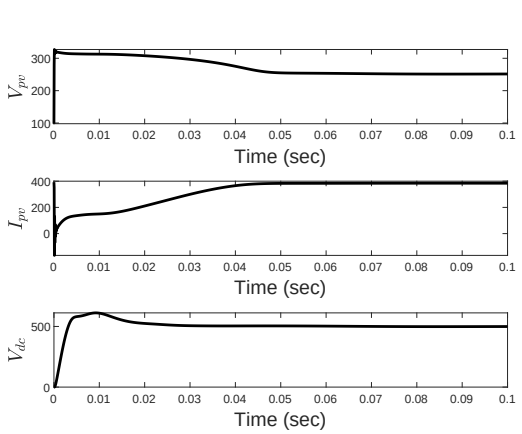
4.3. Case II: Performance of the DSTATCOM with nonlinear and linear load

Figure 11 illustrates the performance evaluation of the PV-fed DSTATCOM with both linear and nonlinear load. The load current before compensation is shown in Figure 11(a), the source current after compensation with IRPT is shown in Figure 11(b). The source current after compensation with the icosϕ algorithm is shown in Figure 11(c). The compensating current with the icosϕ algorithm is shown in Figure 11(d).

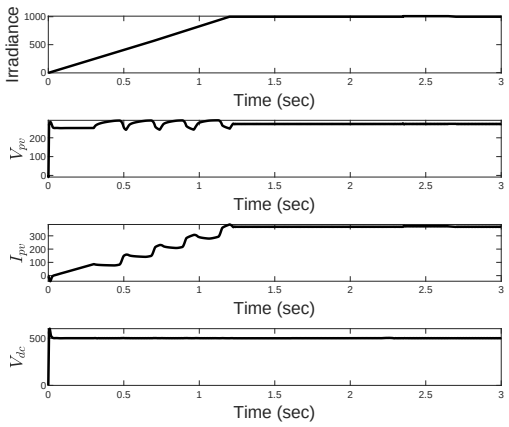
4.4. Case III: Performance of the DSTATCOM with nonlinear load and distorted supply voltage

The performance of the DSTATCOM with distorted supply voltage and nonlinear load is shown in Figure 12 where Figure 12(a) illustrates the distorted supply voltage, Figure 12(b) illustrates the load current before compensation, Figure 12(c) illustrates the source current after compensation, and Figure 12(d) illustrates the compensating current provided by the DSTATCOM.

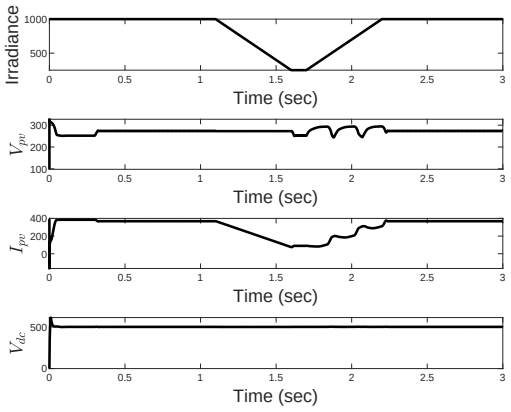
The comparative analysis of the %THD in the source current for different case studies of the SPV-DSTATCOM is shown in Table 4. The uncompensated system has higher %THD whereas the best %THD is provided by the icosϕ control scheme.



(a)



(b)



(c)

Figure 7. (a) DC voltage at uniform irradiance, (b) DC voltage at a ramp increase in solar irradiance, (c) DC bus voltage at non-uniform solar irradiance.

Table 4. Comparative analysis of %THD in source current.

		I_a	I_b	I_c
Case-I	Without compensator	30.92	30.87	30.76
	IRPT	4.79	4.81	4.89
	icosϕ	3.45	3.6	3.52
Case-II	Without compensator	29.45	29.67	29.75
	IRPT	3.81	3.76	3.75
	icosϕ	2.51	2.51	2.44
Case-III	Without compensator	40.18	41.05	40.54
	IRPT	5.71	5.98	5.76
	icosϕ	4.15	4.55	4.61

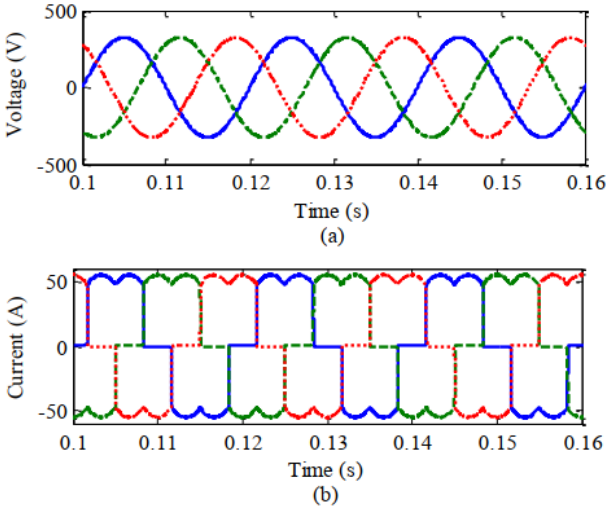


Figure 8. (a) Ideal supply voltage and (b) source current at nonlinear load (before compensation).

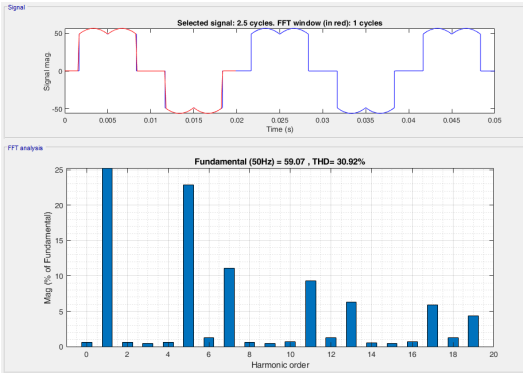


Figure 9. %THD of source current (before compensation).

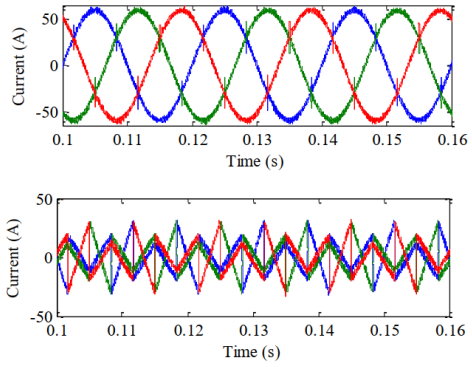


Figure 10. Simulation results of the SPV-fed DSTATCOM with the source current after compensation.

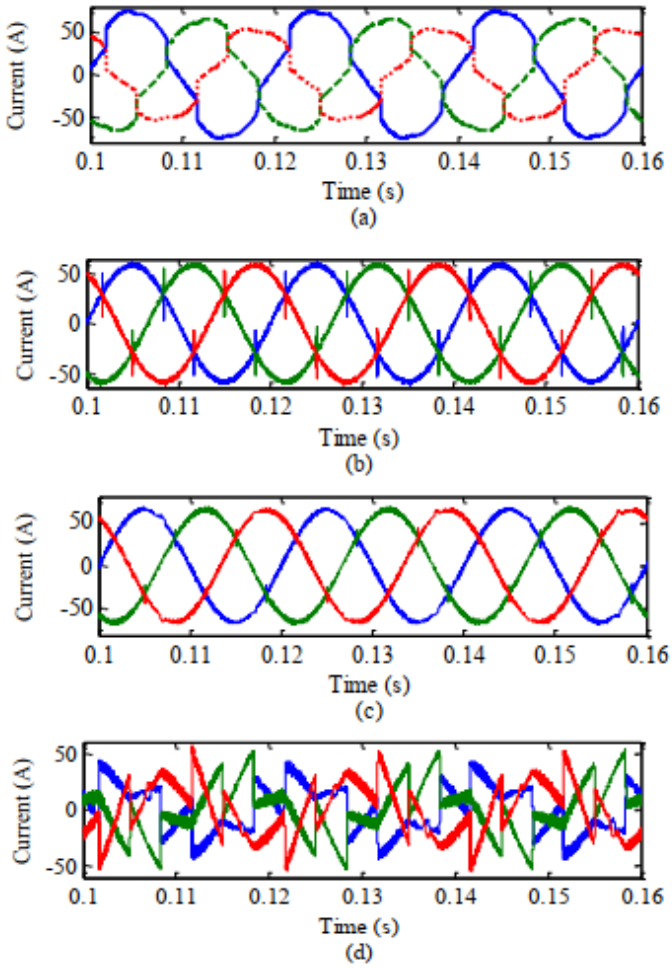


Figure 11. (a) Load current before compensation, (b) source current after compensation using IRPT, (c) source current after compensation using the icosϕ algorithm, (d) compensating current with the icosϕ algorithm.

5. Experimental analysis

The schematic diagram of experimental validation for the SPV-DSTATCOM is shown in Figure 13. The experimental setup is comprised of the following units:

- Power circuit for the QBC-VMC converter and 3-ϕ VSI
- Voltage and current measurement (Hall effect voltage sensor and Hall effect current sensor)
- Nonlinear load (diode bridge rectifier)
- Auxiliary power sources
- dSPACE controller with personal computer
- IGBT driver circuit
- MOSFET driver circuit
- Deadband circuit and isolation circuit

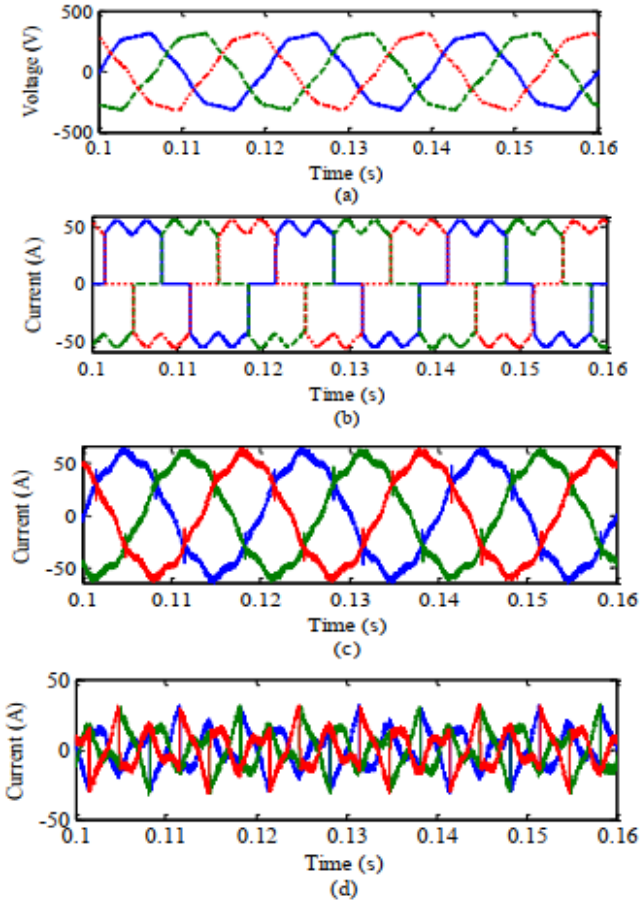


Figure 12. (a) Distorted supply voltage, (b) load current before compensation, (c) source current after compensation, (d) compensating current.

For the experimental validation of the PV-DSTATCOM, six IKW40N120H3 IGBTs are used. The rating of IKW40N120H3 is V_{CE} = 1200 V, I_c = 40 A, and the maximum junction temperature is 175°C. For the MOSFET of the QBC-VMC, STB20NM60 (V_{DS} = 600 V, I_D = 20 A, R_{DS} = 0.25 Ω) is used. For the MOSFET driver MC34151 is used. The voltage and current measurements are carried out using Hall effect sensors LV55 and LA25. The regulated dual power supply of ±15 V is required for the Hall effect sensor. The voltage and current signals are provided to the dSPACE controller. The dSPACE controller digitizes the signals and carries out different computations. For the 3-ϕ IGBT isolated gate driver, 6EDL04I065PRXUMA is used. The different computations carried out in the dSPACE controllers in 1 machine cycle are (a) grid synchronization, (b) reference current generation, (c) voltage controller, (d) SPWM generation, (e) MPPT computation. The experimental results obtained from the experimental setup before and after compensation are shown in Figure 14(a) and Figure 15(a), respectively. For measurement of %THD, power quality analyzer Kusam-Meco KM2100 multifunction power and harmonics analyzer is used. Figure 14(b) and Figure 15(b) illustrate the %THD of the source current before and after compensation.

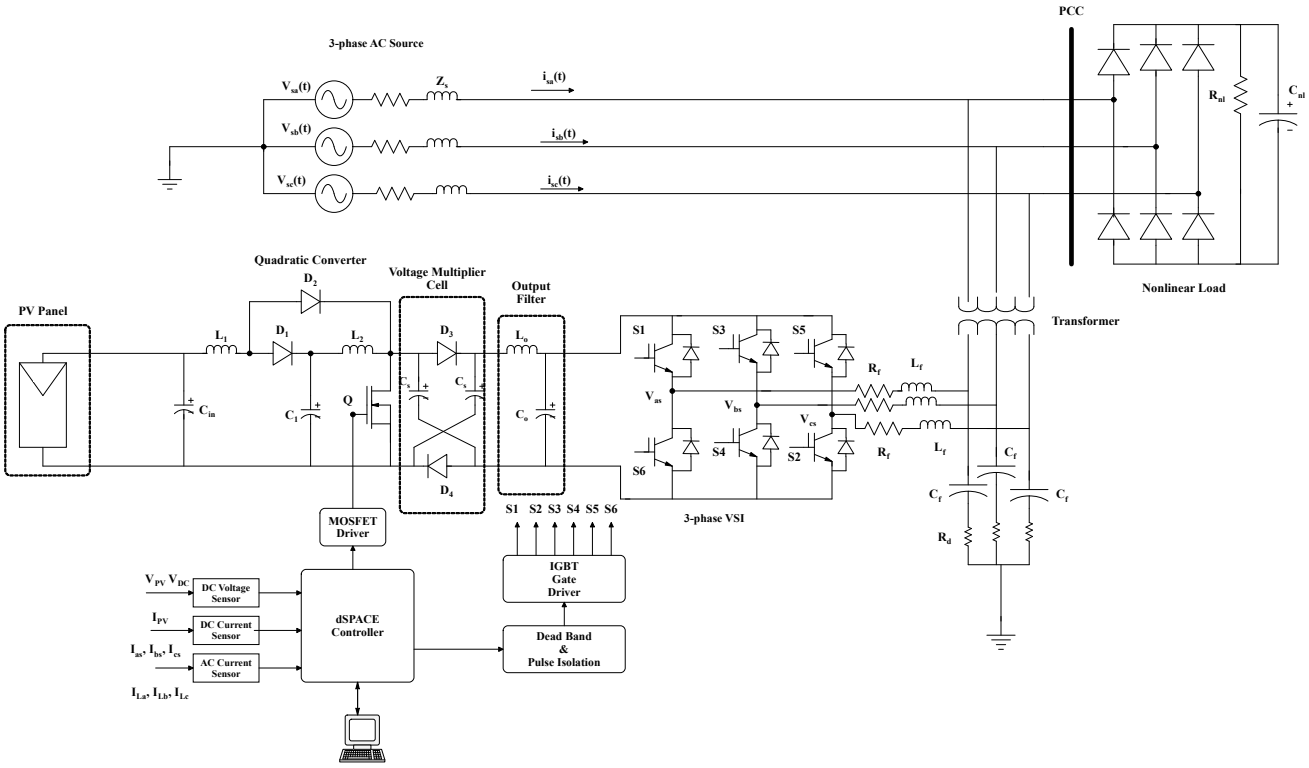
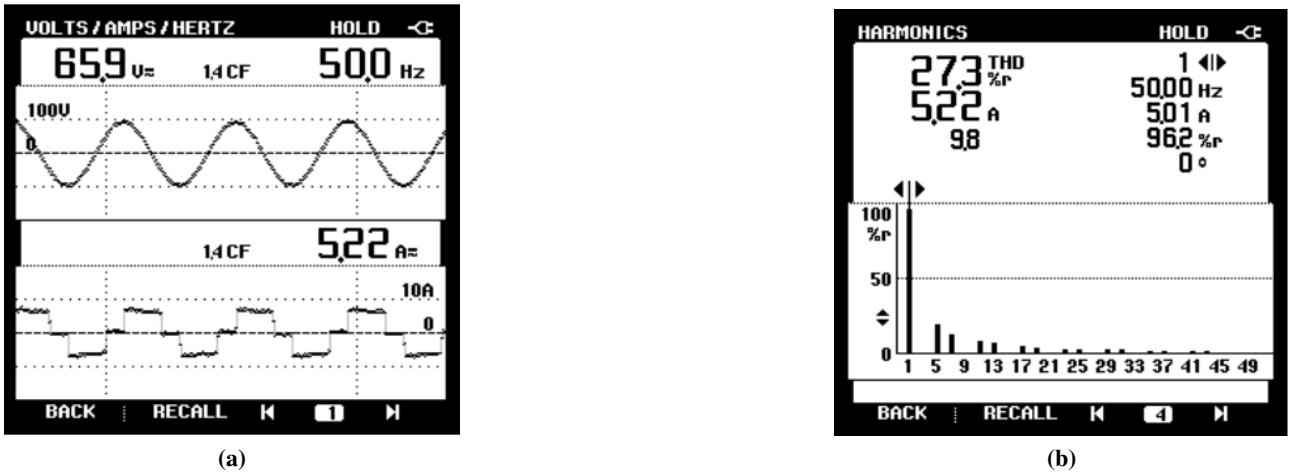
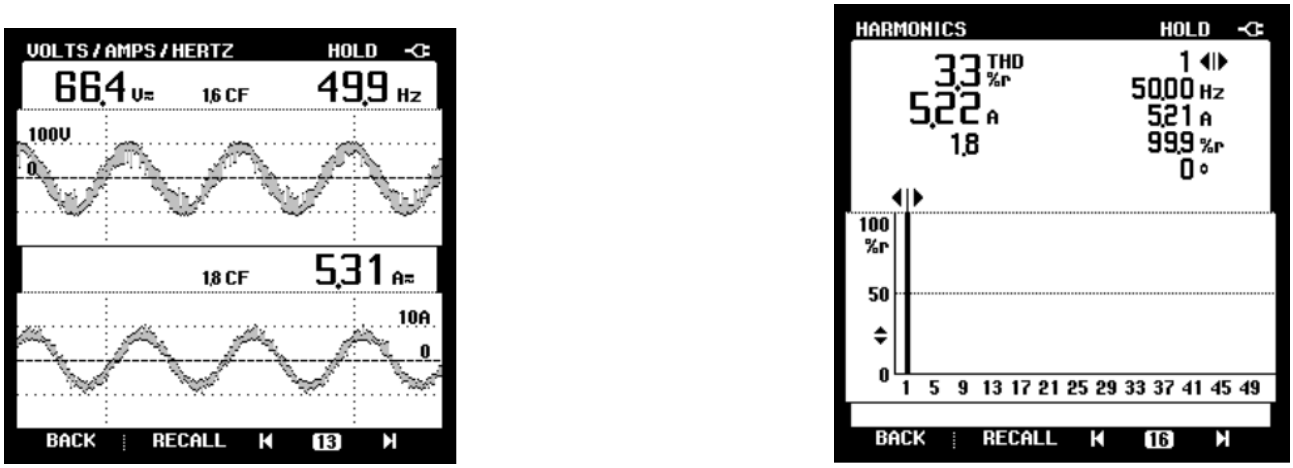


Figure 13. Schematic diagram of the experimental validation of the SPV-DSTATCOM.



(a) **(b)**

Figure 14. (a) Voltage and current before compensation (b) %THD before compensation.



(a) (b)

Figure 15. (a) Voltage and current after compensation (b) %THD after compensation.

6. Conclusions

This paper provides detailed modeling and control aspects of the grid-integrated SPV-DSTATCOM. A detail operation of the SPV-DSTATCOM has been provided with limits of the reactive power in the power system as well as different mode of operations of the SPV-DSTATCOM. The two-stage PEI is comprised of the QBC-VMC converter and DSTATCOM. The QBC-VMC converter is controlled using the variable step size MPPT algorithm. The icosϕ algorithm is used for the reference current and unit template generation for DSTATCOM control. The PI controller is used for DC and AC voltage control. Different case studies are considered and simulation results have been provided. From the simulation results it can be found out that the DSTATCOM is able to provide reactive power compensation as well as harmonic mitigation in different case studies. To validate the simulation results, experimental analysis is provided.

Author contributions

Tarun Naruka: Conceptualization, Software, Investigation, Writing – original draft, Writing – review and editing; Debasis Tripathy: Writing – original draft; Prangya Mohanty: Software, Investigation. All authors have read and agreed to the published version of the manuscript.

Use of Generative-AI tools declaration

The authors declare that they have not used any Artificial Intelligence (AI) tools in the creation of this article.

Conflict of interest

All authors declare no conflicts of interest in this paper.

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