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Research article

Analytical subthreshold swing model of junctionless elliptic gate-all-around (GAA) FET

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Abstract: An analytical subthreshold swing (SS) model has been presented to determine the SS of an elliptic junctionless gate-all-around field-effect transistor (GAA FET). The analysis of a GAA FET with an elliptic cross-section is essential because it is difficult to manufacture a GAA FET with an accurate circular cross-section during the process. The SS values obtained using the proposed SS model were compared with 2D simulation values and other papers to confirm good agreement. Using this analytical SS model, SS was analyzed according to the eccentricity of the elliptic cross-section structure. As a result, it was found that the carrier control ability within the channel improved as the eccentricity increased due to a decrease in the effective channel radius by a decrease in the minor axis length and a decrease in the minimum potential distribution within the channel, and thus the SS decreased. There was no significant change in SS until the eccentricity increased to 0.75 corresponding to the aspect ratio (AR), the ratio of the minor and major axis lengths, of 1.5. However, SS significantly decreased when the eccentricity increased to 0.87 corresponding to AR = 2. As a result of the SS analysis for changes in the device parameters of the GAA FET, changes in the channel length, radius, and oxide film thickness significantly affected the changing rate of SS with eccentricity.

Keywords: elliptic; gate-all-around (GAA); subthreshold swing; eccentricity; aspect ratio

1. Introduction

The increase in leakage current in the subthreshold region due to the decrease in transistor size

is becoming an obstacle to manufacturing large-scale integrated circuits (ICs). In addition, efforts are being made to improve output characteristics by developing transistor structures and materials for high-speed operation and low-power characteristics [1,2]. To solve this problem, gate-all-around (GAA) FET has recently been attracting attention as the most ideal device [3,4]. Samsung and TSMC are also competing in developing ICs with GAA FETs, and microstructure GAA FETs are receiving a lot of attention to compete for leadership in the semiconductor industry in the future [5,6]. Meanwhile, active research has been conducted on GAA FETs according to the cross-section structure of the channel [7–9]. Research on the circular structure has been actively conducted due to problems arising from the edge effect of the square structure. Still, the problem has arisen that it is difficult to implement a channel structure with a circular cross-section in real fabrication [10–12]. In actual fabrication, the size in the lateral direction is determined by lithography, and the dimension in the vertical direction is determined by the film thickness of the silicon. Since the oxidation reaction is different in each direction, forming a channel with an exact circular structure will not be possible. Therefore, a GAA nanowire FET showing a channel cross-sectional area of mostly elliptical structure will be formed even if the process is done to have a circular cross-section. Nevertheless, many studies have been conducted to interpret the GAA FET as having the cross-sectional area of the circular structure [13,14]. However, research on elliptic GAA FETs was also conducted, and it was focused only on the analysis of short channel effects (SCEs) for the geometric aspect ratio (AR), which is the ratio of the major and minor axis [15,16].

In particular, when analyzing the elliptic GAA FET, the effective radius of the elliptic cross-section was simply calculated and the SCEs of the elliptic GAA FET were analyzed using the potential distribution model obtained from the existing circular GAA FET [17,18]. Saha et al. presented a drain current model of an elliptic GAA heterojunction tunnel FET [19]. Chiang presented a subthreshold current model that could include interface-trapped-charge for an elliptic GAA FET but focused on logic swing [20].

Looking at various papers analyzing the SCEs on the geometric impact of elliptic GAA FETs, the changes in drain current, DIBL, subthreshold swing, etc., according to AR were mentioned. However, most of these papers fixed the length of the major or minor axis and changed the size of the remaining axis to examine changes in SCEs in response to changes in AR [21]. The problem here is that the cross-sectional area of the channel changes if the length of the major or minor axis is fixed and the size of the remaining axis is changed. In this case, the subthreshold characteristics will naturally change. Therefore, in this paper, the change in subthreshold swing was observed when AR changed in an elliptic GAA FET with the same cross-sectional area as a circular GAA FET.

Many papers used junction-based structures to analyze the SCEs of elliptic GAA FETs [22–24]. However, as the channel length becomes shorter, the junction-based structure is showing limitations in the existing metal-oxide-semiconductor field-effect transistor (MOSFET) process due to the rapid change in doping concentration that occurs between the source/drain region and the channel [25–27]. The transistor structure designed to solve this problem is the junctionless MOSFET. The junctionless MOSFETs have the advantage of a simple process because there is no junction between the source/drain and the channel, which not only reduces process costs but also allows the process of the conventional MOSFETs [28]. Liao et al. and Scarlet et al. analyzed the SCEs of junctionless elliptic FETs, but only analyzed on and off currents [29–30]. In this paper, we have presented an analytical SS model of a junctionless elliptic GAA FET according to the eccentricity of an elliptic GAA FET with the same cross-sectional area.

2. Subthreshold swing of a junctionless elliptic GAA FET

2.1. Structure of junctionless elliptic GAA FET

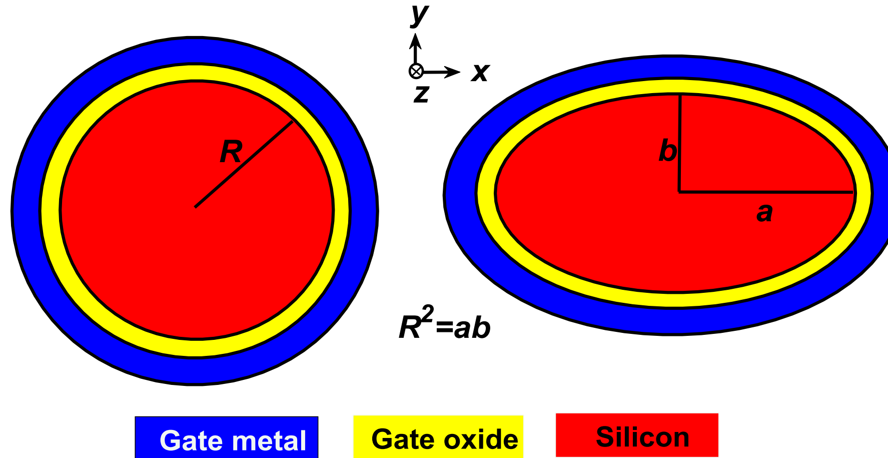

Figure 1. Cross-sectional view of a junctionless circular and elliptic GAA FET.

Figure 1 is a cross-sectional structure of the GAA FET used in this paper. As shown in Figure 1, the SS is obtained when the a and b change using the length a of the major axis and the length b of the minor axis for an elliptic GAA FET with the same channel cross-sectional area as the circular GAA FET. The channel material is silicon, and the gate oxide film is SiO_2. The doping concentration of the channel was 10^{19}/cm^3. The device parameters used in this paper are listed in Table 1.

Table 1. Device parameters for this analytical SS model.

Device parameter	Symbol	Value
Channel length	L_g	10~60 nm
Channel radius	R	5~10 nm
Oxide thickness	t_{ox}	1~5 nm
Doping concentration	N_d	10^{19} /cm^3
Eccentricity	e	0~0.99

To compare the circular and elliptic GAA FETs with the same cross-sectional area, the channel cross-sectional area of the circular FET (πR^2) and the cross-sectional area of the elliptic FET (πab) were set to be the same. At this time, the relationship between the eccentricity of the ellipse, the major and minor axis lengths, and AR can be expressed as (2.1).

$$\begin{aligned} &e = \sqrt{1-\left(\frac{b}{a}\right)^2} = \sqrt{1-\left(\frac{1}{AR}\right)^2} \\ &AR = 1/\sqrt{1-e^2} \\ &a = b \times AR,\ b = R/\sqrt{AR},\ R^2 = ab \end{aligned} \tag{2.1}$$

In (2.1), the AR represents the aspect ratio (=*a/b*). In this paper, Chaing's junction-based potential model was modified to obtain the potential distribution within the channel of the junctionless elliptic GAA FET [20]. In other words,

$$\phi(x,y,z)=\phi_C(z)+\left(\frac{x^2}{2\lambda_a^2}+\frac{y^2}{2\lambda_b^2}\right)\left\{\left(V_{gs}-V_{fb}\right)-\phi_C(z)\right\} \tag{2.2}$$

Here, V_{gs} and V_{fb} represent the gate voltage and flat band voltage, respectively. $\phi_C(z)$ is the potential of the central axis obtained along the channel length direction as in (2.3).

$$\begin{cases}\dfrac{d^2\phi_C(z)}{dz^2}+\dfrac{\phi_C(z)-\varphi_{CL}}{\lambda^2}=0\\ \varphi_{CL}=V_{gs}-V_{fb}+\dfrac{qN_D\lambda^2}{\varepsilon_{si}}\end{cases} \tag{2.3}$$

The φ_{CL} represents the long channel central potential, and λ represents the scaling length. The scaling length is given as:

$$\frac{1}{\lambda^2}=\frac{1}{\lambda_a^2}+\frac{1}{\lambda_b^2} \tag{2.4}$$

where λ_a and λ_b are the scaling lengths of the elliptic GAA FET for the major and minor axis, respectively, and are:

$$\begin{cases}\lambda_a^2=\dfrac{2a\varepsilon_{si}+C_{ox}a^2}{2C_{ox}}\\ \lambda_b^2=\dfrac{2b\varepsilon_{si}+C_{ox}b^2}{2C_{ox}}\\ C_{ox}=\dfrac{\varepsilon_{ox}}{t_{ox_eff}}\\ t_{ox_eff}=R_{eff}\left(1+\dfrac{t_{ox}}{R_{eff}}\right)\end{cases} \tag{2.5}$$

The C_{ox} is the effective capacitance per unit area of the gate oxide film, and ε_{ox} and ε_{si} represent the dielectric constants of SiO_2 and Si, respectively. The t_{ox_eff} is the effective gate oxide film thickness. In (2.5), R_{eff} is the effective radius of the circle when the ellipse is assumed to be a circle and can be obtained from (2.6) [14,18].

$$\frac{4\varepsilon_{ox}}{2\varepsilon_{si}R_{eff}t_{ox}+\varepsilon_{ox}R_{eff}^2}=\frac{2\varepsilon_{ox}}{2\varepsilon_{si}at_{ox}+\varepsilon_{ox}a^2}+\frac{2\varepsilon_{ox}}{2\varepsilon_{si}bt_{ox}+\varepsilon_{ox}b^2} \tag{2.6}$$

Many papers used approximation equations according to the sizes of *a*, *b*, and t_{ox}, but in this paper, the exact R_{eff} was obtained using MATLAB's *solve* command.

2.2. Analytical SS model for a junctionless elliptic GAA FET

The SS is a measure of the reduction of leakage current below the threshold voltage and can be obtained using the slope of the relationship between the drain current and gate voltage in the subthreshold region. This can ultimately be derived from the relationship between the gate voltage and potential [31,32]. According to the definition of subthreshold swing, the SS can be obtained as in (2.7).

$$SS = \frac{dV_{gs}}{d(\log I_{ds})} = \ln(10)\left(\frac{kT}{q}\right)\left(\frac{d\phi_{C\min}}{dV_{gs}}\right)^{-1} \tag{2.7}$$

Here, $\phi_{C\min}$ represents the minimum value of the central potential distribution obtained in (2.3). In other words, based on the 1D ordinary differential equation, the central potential in (2.3) is:

$$\phi_C(z) = Ae^{-\frac{z}{\lambda}} + Be^{\frac{z}{\lambda}} + \varphi_{CL} \tag{2.8}$$

Using the boundary condition $\phi_C(z=0) = V_{bi}$, $\phi_C(z=L_g) = V_{bi} + V_{ds}$ (here, V_{ds} is the drain voltage and V_{bi} is the junction potential of the source/drain), the constants *A* and *B* are obtained as in (2.9).

$$A = \frac{\left(V_{bi} - \varphi_{CL}\right)\left(e^{\frac{L_g}{\lambda}} - 1\right) - V_{ds}}{2\sinh\left(\frac{L_g}{\lambda}\right)},\ B = \frac{V_{ds} - \left(V_{bi} - \varphi_{CL}\right)\left(e^{-\frac{L_g}{\lambda}} - 1\right)}{2\sinh\left(\frac{L_g}{\lambda}\right)} \tag{2.9}$$

Here, we found the minimum z_{min} from the derivative of (2.8), and the minimum potential value can be obtained as in (2.10).

$$\begin{aligned} \phi_{C\min}(z = z_{\min}) &= 2\sqrt{AB} + \varphi_{CL} \\ z_{\min} &= \frac{\lambda}{2}\ln\left(\frac{A}{B}\right) \end{aligned} \tag{2.10}$$

The expression in the second parenthesis on the right side of (2.7) is:

$$\begin{aligned} \frac{d\phi_{C\min}}{dV_{gs}} &= \frac{d}{dV_{gs}}\left\{2\sqrt{AB} + \varphi_{CL}\right\} = 2\frac{d\sqrt{AB}}{dV_{gs}} + \frac{d\varphi_{CL}}{dV_{gs}} = 2\frac{d\sqrt{AB}}{dV_{gs2}} + 1 \\ &= \left\{-(e^{\frac{L_g}{\lambda}} - 1)\sqrt{\frac{B}{A}} + (e^{\frac{-L_g}{\lambda}} - 1)\sqrt{\frac{A}{B}}\right\} / 2\sinh\left(\frac{L_g}{\lambda}\right) + 1 \end{aligned} \tag{2.11}$$

By substituting (2.11) into (2.7), the SS of the junctionless elliptic GAA FET can be obtained analytically. It can be seen that the first and second terms in the parentheses of (2.11) are always negative. Therefore, $d\phi_{C\min}/dV_{gs}$ is always less than 1, so as can be seen in (2.7), it can be found that the SS value is always greater than ln(10)(kT/q) ≈ 60 mV/dec.

3. Validity of analytical SS model for a junctionless elliptic GAA FET

3.1. Validity of analytical SS model

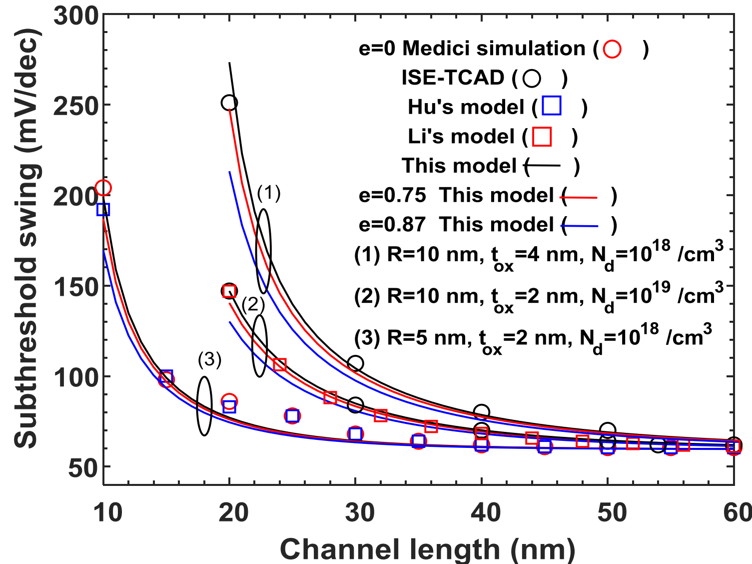

Figure 2. Comparisons of subthreshold swings of this model with the results of TCAD and Medici simulation from other papers.

To validate the analytical SS model for the junctionless elliptic GAA FET obtained in (2.7), the results of other papers [31,33] were compared in Figure 2. As shown in Figure 2, the analytical SS model presented in this paper matched well with the results of other papers. Therefore, we will analyze the junctionless elliptic GAA FET using the analytical SS model derived in Section 2.2. In Figure 2, it can be seen that SS decreased as the eccentricity increased. Eccentricity e = 0.75 corresponded to AR = 1.5, and e = 0.87 corresponded to AR = 2. As eccentricity increased, it became a GAA FET with a cross-sectional area closer to an ellipse, and at this time, the reason why SS decreased will be explained.

The central electrostatic potential obtained using (2.8) is shown with eccentricity as a parameter in Figure 3. As shown in Figure 3, a large eccentricity of elliptic GAA FET led to better electrostatic potential distribution, thus better short-channel performance, because the current flowing in the subthreshold region decreased if the central electrostatic potential decreased. The change in minimum potential for the gate voltage change is shown in the inset of Figure 3. As can be seen by observing the size of the arrow in the case of e = 0.2 and e = 0.9 in the figure, the change in minimum potential increased with the increase in eccentricity for the gate voltage change, which will appear as a decrease in SS.

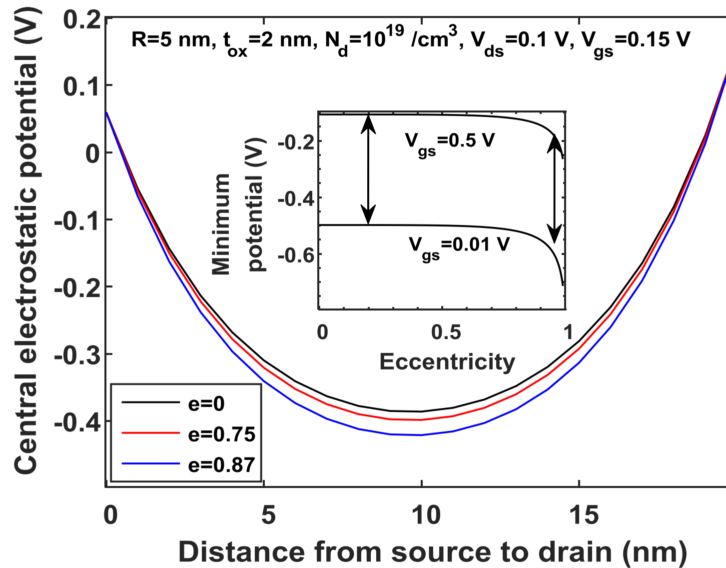

Figure 3. Central electrostatic potential distributions with different eccentricity under the given conditions in the figure.

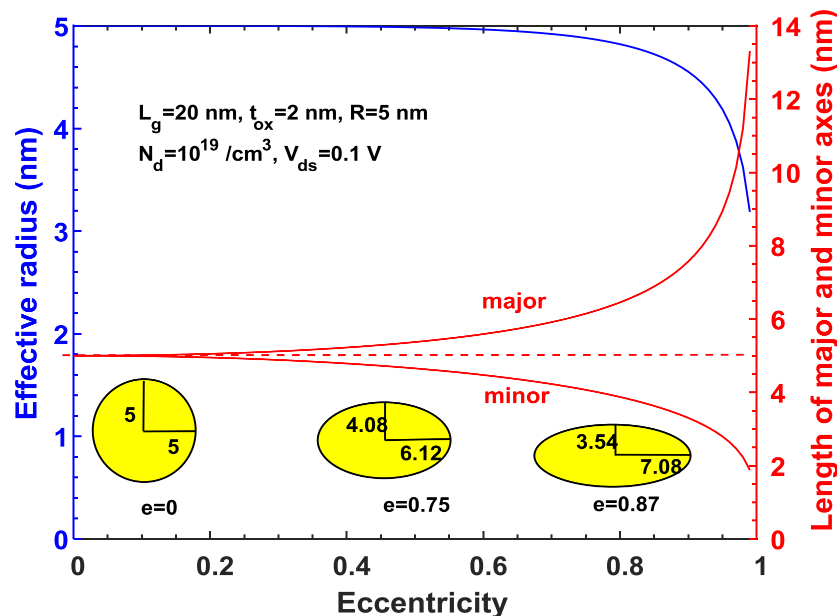

Figure 4. Effective radius and length of major and minor axes for the eccentricity of the elliptic GAA FET under the conditions given in the figure.

The change according to the eccentricity of R_{eff} obtained in (2.6) is shown in Figure 4 along with the change in a and b. As can be seen in the inset of the figure, the circular cross-section area and elliptic cross-section area were set to be the same and the results were plotted according to (2.1) and (2.6). As shown in Figure 4, as the eccentricity increased, that is, from a circle to an ellipse, R_{eff} decreased, and when the eccentricity was over 0.8, R_{eff} decreased sharply. Additionally, as eccentricity increased, the length of the major axis rapidly increased and the length of the minor axis rapidly decreased. A decrease in the length of the minor axis ultimately resulted in a decrease in R_{eff}, which shows that the control ability of the carrier within the channel of the gate voltage was improved. In other words, when the cross-sectional area changed to an oval shape, it was seen that

the length of the minor axis affected SS more than the major axis.

As shown in Figure 4, the length of the minor axis had a greater influence on the ability to control carriers within the channel by gate voltage. To examine in more detail the effect of the lengths of the major and minor axes on SS, Figure 5 shows the change in transverse potential distributions in the major and minor axes directions at $z = z_{min}$. As shown in Figure 5, the potential distribution in the major and minor directions simultaneously decreased as e increased. However, it can be seen that there was a difference in the potential distribution for the directions of the major and minor axes. In other words, the potential distributions in the minor axis direction decreased as eccentricity increased in all areas, but those in the major axis direction decreased in the center of the channel, but increased toward the edge of the channel as eccentricity increased. As explained in Figure 3, it can be predicted that the current level increases in the subthreshold region, short channel performance decreases, and SS increases as the potential distribution increases. Therefore, it can be seen that not only does the SS reduce due to the decrease in the length of the minor axis, but also the SS increases due to the increase in the length of the major axis, which occurs simultaneously as eccentricity increases. However, due to the nature of the junctionless FET, most channel carriers flow through the center, so the potential distribution in the center is important. Therefore, it can be predicted that SS will decrease as e increases.

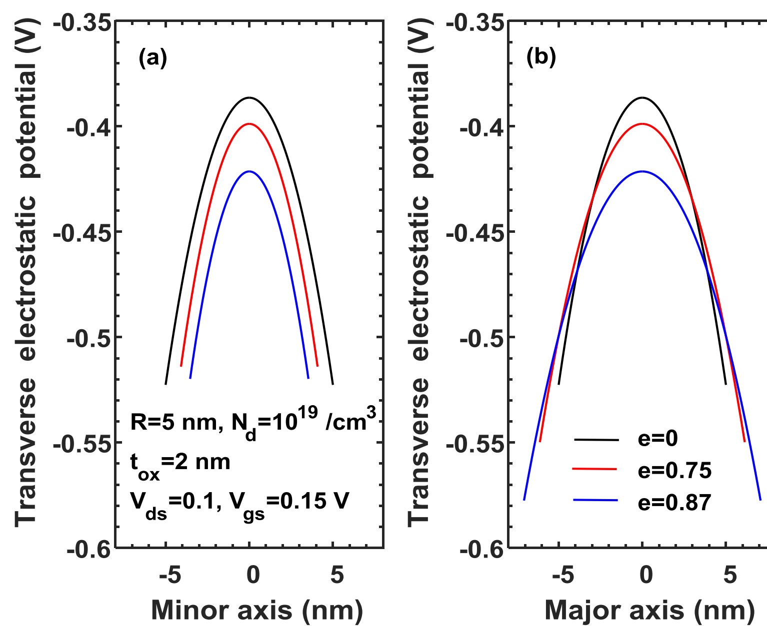

Figure 5. Transverse electrostatic potential distribution at $z = z_{min}$ for (a) minor axis and (b) major axis under the given conditions in the figure.

3.2. Subthreshold swing for the device parameters of a junctionless elliptic GAA FET

The changes in SS were observed for changes in the device parameters of the junctionless elliptic GAA FET used in Table 1. First, using (2.11), the change of $\phi_{C\min}$ for the gate voltage (i.e., the change in the arrow size for the gate voltage shown in the inset of Figure 3) is shown in Figure 6 with the channel length as a parameter. As shown in Figure 6, it shows an almost constant value regardless of the channel length when the eccentricity was less than 0.8. However, in the region of $e > 0.8$, there was a significant change as the channel length became smaller. Ultimately, SS also saw

big changes in this area. When the channel length increased to L_g = 50 nm or more, it was observed that there was almost no change for the eccentricity. As shown in Figure 6, it was observed that the change in SS could not be ignored as the channel length became shorter and the eccentricity increased beyond $e > 0.8$.

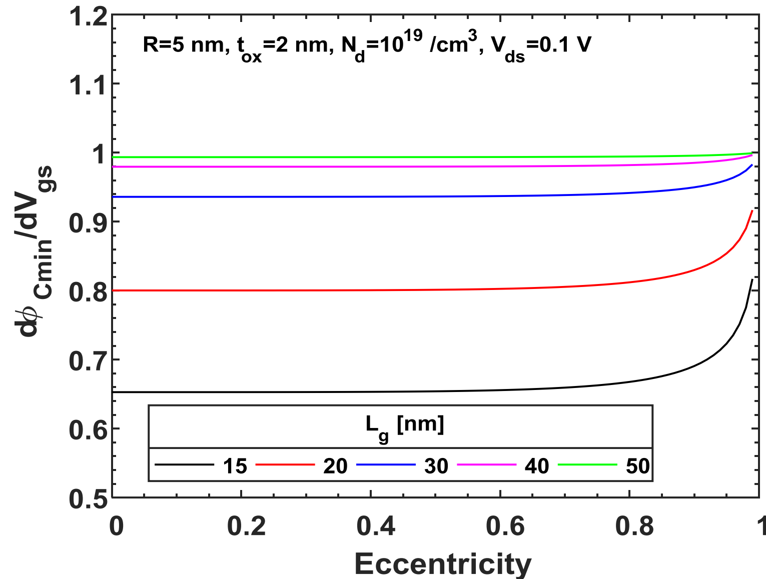

Figure 6. Differentiation of $\phi_{C\min}$ for V_{gs} for the eccentricity with channel length as a parameter under the given conditions in the figure.

The SS, calculated with the channel length as a parameter using (2.7), is shown in Figure 7. Figure 7 has an inverse relationship with Figure 6 according to (2.7). As mentioned above, the length of the minor axis had a greater impact on subthreshold performance than the length of the major axis, and the length of the minor axis decreased as the eccentricity increased in Figure 4, and thus SS also decreased. In particular, it was observed that SS changed very sensitively due to changes in the eccentricity as the channel length became shorter, and eccentricity has had little effect on SS when the channel length is was over 40 nm. In other words, as the channel length becomes shorter, the deformation of the cross-section of the circular GAA FET that may occur during the manufacturing process will have a significant impact on SS. SS values according to channel length and eccentricity under the conditions given in Figure 7 are shown in Table 2.

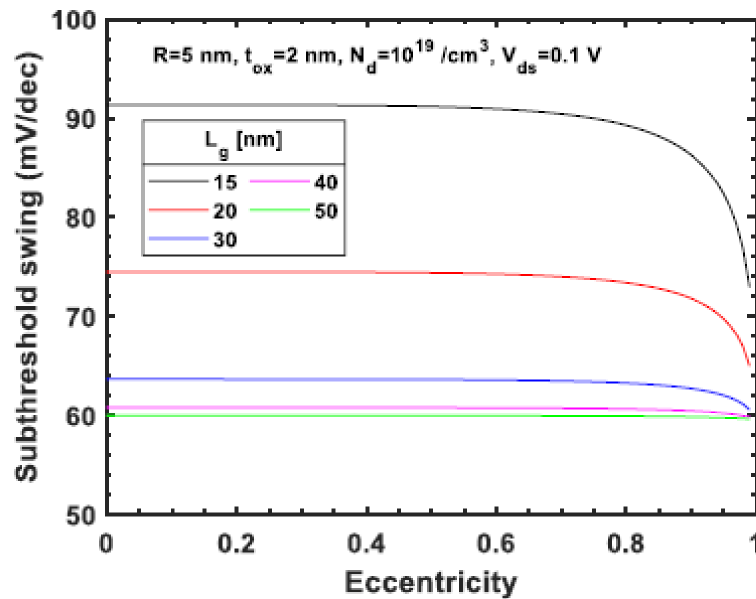

Figure 7. Subthreshold swings for the eccentricity with channel length as a parameter under the given conditions in the figure.

Table 2. SSs for channel length and eccentricity under the given conditions in Figure 7.

Channel length [nm]	Eccentricity	SS [mV/dec]
15	0.5	91.2
	0.75	90.0
	0.87	87.6
20	0.5	74.4
	0.75	73.8
	0.85	72.5
30	0.5	63.6
	0.75	63.4
	0.87	63..0
40	0.5	60.8
	0.75	60.7
	0.87	60.6
50	0.5	60.0
	0.75	60.0
	0.87	60.0

In general, the channel diameter must be shorter than the channel length, and the quantum effect must be considered at $R < 5$ nm, so the change in SS and the change of the minimum potential for gate voltage according to eccentricity at 5 nm < R < 9 nm are shown in Figures 8(a) and (b) in the range to be able to ignore this effect when L_g = 20 nm. The SS also increased due to the decrease of the change of the minimum potential for gate voltage as R increased in the circular GAA FET of $e = 0$. As the eccentricity increased and the ellipse became flatter, SS decreased regardless of the channel radius, and the larger the channel radius, the more the reduction rate of SS increased as eccentricity increased. As shown in Figure 4, as eccentricity increased, R_{eff} decreased, and

eventually, λ became smaller due to $\lambda < R$. As can be seen from (2.3) and (2.9), if λ becomes smaller, the rate of change for V_{gs} of A and B will increase, and the rate of the change of the minimum potential for gate voltage will also increase, so eventually, the rate of change in SS will also increase. SS values according to channel radius and eccentricity under the conditions given in Figure 8 are shown in Table 3.

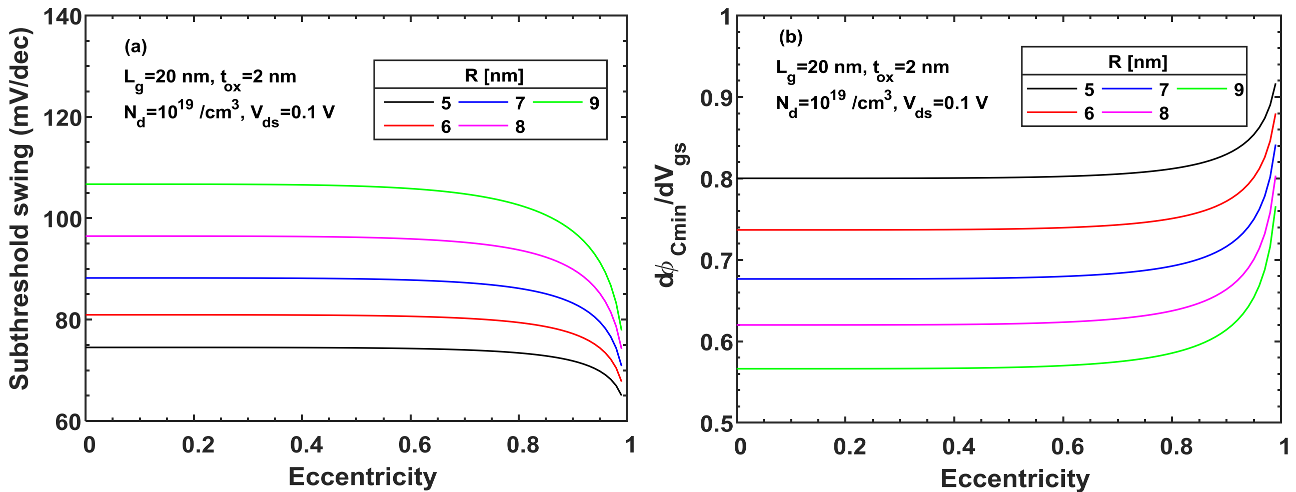

Figure 8. (a) Subthreshold swings and (b) the change of minimum potential for gate voltage for the eccentricity with channel radius as a parameter under the given conditions in the figure.

Table 3. SSs for channel radius and eccentricity under the given conditions in Figure 8.

Channel radius [nm]	Eccentricity	SS [mV/dec]
5	0.5	74.4
	0.75	73.8
	0.87	72.5
6	0.5	80.8
	0.75	79.9
	0.85	78.1
7	0.5	88.0
	0.75	86.9
	0.87	84.5
8	0.5	96.2
	0.75	94.6
	0.87	91.5
9	0.5	106.3
	0.75	103.9
	0.87	99.5

The decrease in R_{eff} due to the increase in eccentricity affects not only the decrease in SS but also the central electrostatic potential. To investigate this, the central electrostatic potential distribution at e = 0 and e = 0.87 was plotted in Figure 9, when the channel length was fixed at 20 nm and the channel radius R was increased from 5 nm to 9 nm. As shown in Figure 9, the potential

distribution increased as the channel radius increased, which appeared as an increase in SS due to the degradation of short channel performance as mentioned above. In addition, the central electrostatic potential distribution decreased significantly for a relatively large radius as the eccentricity increased, so it can be seen that the SS value also decreased significantly.

To observe the SS of the junctionless elliptic GAA FET according to the thickness of SiO_2 among device parameters, the SS according to eccentricity is shown in Figure 10 with the thickness of SiO_2 as a parameter. As shown in Figure 10, the SS changed significantly depending on the oxide film thickness, and SS also increased as the oxide film thickness increased like a circular GAA FET. This is because the electric field formed by the gate voltage is hindered from reaching the channel through the gate metal as the thickness of the oxide film increases. In addition, SS also decreased as eccentricity increased, and it can be observed that SS decreased to a greater extent as eccentricity increased and the oxide film thickness increased. SS values according to oxide thickness and eccentricity under the conditions given in Figure 10 are shown in Table 4.

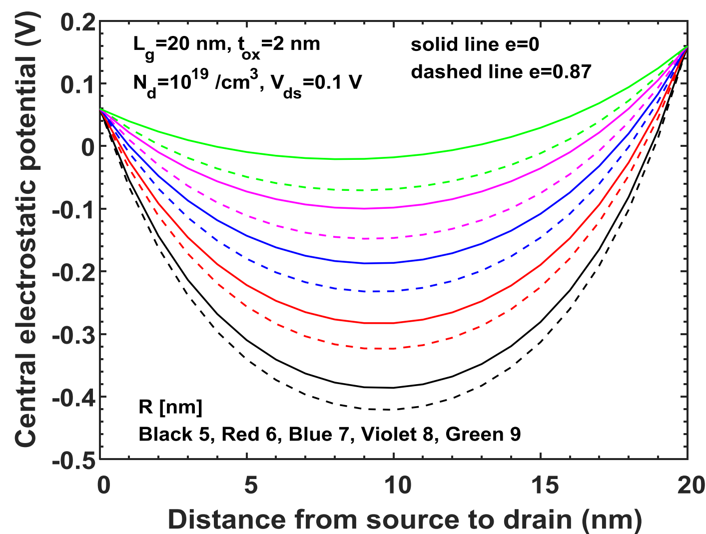

Figure 9. Central electrostatic potential distributions with the channel radius and eccentricity as parameters under the given conditions in the figure.

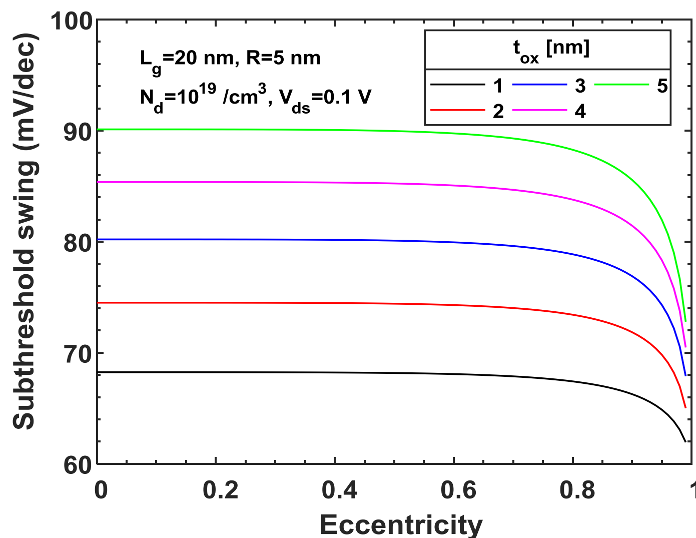

Figure 10. Subthreshold swings for the eccentricity with gate oxide thickness as a parameter under the given conditions in the figure.

Table 4. SSs for oxide thickness and eccentricity under the given conditions in Figure 10.

Oxide thickness [nm]	Eccentricity	SS [mV/dec]
1	0.5	68.2
	0.75	67.7
	0.87	66.8
2	0.5	74.4
	0.75	73.8
	0.85	72.5
3	0.5	80.1
	0.75	79.3
	0.87	77.7
4	0.5	85.2
	0.75	84.3
	0.87	82.4
5	0.5	90.0
	0.75	88.9
	0.87	86.7

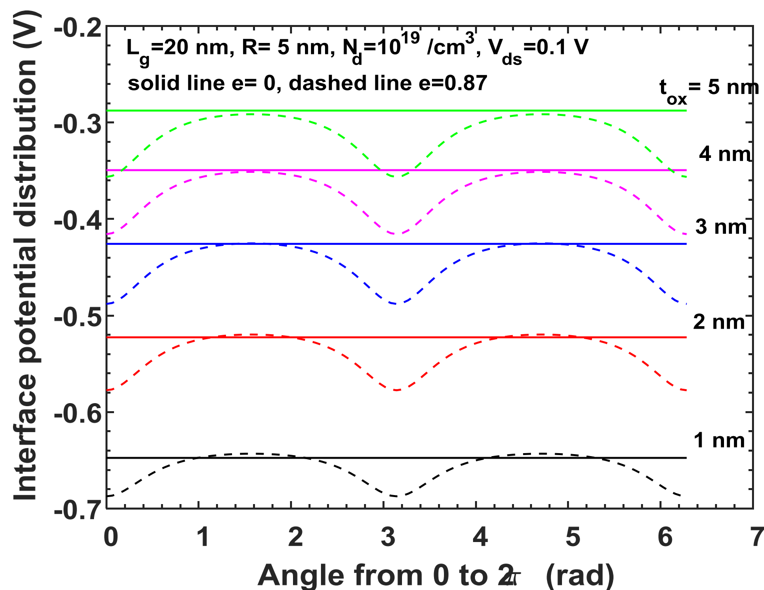

Figure 11. Potential distributions at Si/SiO2 interface from 0 to 2π with gate oxide as a parameter under the given conditions in the figure.

As mentioned above, to investigate the potential distribution at the Si/SiO_2 interface that affects the electric field within the channel as the oxide film thickness increases, the potential distribution at the interface is shown in Figure 11 with the oxide film thickness as a parameter. As shown in Figure 11, the circular GAA FET naturally showed the same potential distribution at all interfaces, but at $e = 0.87$, that is, when the length of the major axis was twice the minor axis length, the potential distribution at all interfaces decreased compared to the circular GAA FET. The control ability of the carriers in the channel according to the gate voltage in the subthreshold region improved if the

potential decreased, and the SS decreased. In other words, as can be seen in Figure 10, as eccentricity increased, SS decreased. As the oxide film thickness increased, the potential distribution further decreased, so it can be observed that SS also rapidly decreased. As can be seen in Figure 5, the potential at the end of the minor axis was higher.

4. Conclusions

In the case of a junctionless elliptic GAA FET, SS was analyzed and compared with a circular GAA FET. For this purpose, an analytical SS model was presented, and good agreement was observed by comparing the results of the simulation using 2D potential distribution and the results of other papers. The SS was compared when the cross-section changed from circular to elliptic and had the same area, and the change in SS was observed with respect to the change in eccentricity of the ellipse. Because it is difficult to manufacture a perfectly circular structure during the process, research on GAA FETs with an elliptic cross-section is very important. As a result, it was observed that SS decreased as eccentricity increased, but there was no significant change in SS until AR was about 1.5, i.e., e = 0.75. However, when AR increased to 2 corresponding to e = 0.87, a significant change in SS was observed. This was due to changes in the potential distribution in the minor and major axes and a decrease in R_{eff} as eccentricity increased. As eccentricity increased, the minimum potential in the channel decreased, and the rate of change of minimum potential according to the gate voltage increased, thereby improving the control ability of the gate voltage over the carriers in the channel. As eccentricity increased, the control ability of carriers in the channel by gate voltage was improved by decreasing the minor axis length rather than the major axis length. This effect almost did not appear when the channel length increased up to 50 nm, and the change in SS due to the increase in eccentricity was decreased as the channel radius and the oxide film thickness decreased. In the future, using this potential distribution model, we will study the threshold voltage and drain-induced barrier lowering, and the case of using ferroelectric as an oxide film. In addition, research should be conducted on oxide film materials and channel structures that can more effectively control carriers in the channel of the elliptic structure that appear indispensable in the process.

Use of AI tools declaration

The authors declare that they have not used artificial intelligence (AI) tools in the creation of this article.

Conflict of interest

The author declares that there are no conflicts of interest in this paper.

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