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Research article

Analysis of drain induced barrier lowering for junctionless double gate MOSFET using ferroelectric negative capacitance effect

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Abstract: We analyze the drain induced barrier lowering (DIBL) of a negative capacitance (NC) FET using a gate structure such as a metal-ferroelectric-metal-insulator-semiconductor (MFMIS) for a junctionless double gate (JLDG) FET. NC FETs show negative DIBL characteristics according to the ferroelectric thickness. To elucidate the cause of such negative DIBL, the DIBLs are obtained by the second derivative method using the 2D potential distribution and drain current-gate voltage curve. The analytical DIBL model is also presented for easy observation of the DIBL of NC FET. It has been found that the results of this analytical DIBL model are very similar to those of the second derivative method. The results of this analytical DIBL model are also in good agreement with the results of TCAD. As a result, it was found that the negative DIBL phenomenon is caused by the change according to the drain voltage of the charge existing in the ferroelectric material. The negative DIBL phenomenon easily occurred as the ferroelectric thickness increased and the thickness of SiO_2 used as an insulator decreases.

Keywords: drain induced barrier lowering; junctionless; ferroelectric; negative capacitance; double gate

1. Introduction

With decreasing transistor size, the short channel effects become more serious, and various

three-dimensional transistors have been developed and used to overcome these obstacles, such as FinFETs and GAA (Gate-All-Around) structures [1–6]. In addition to the multi-gate structure, the gate engineerings are being conducted to reduce the short-channel effect [7–9]. However, since the short-channel effect cannot be completely eliminated even in these various three-dimensional structures, a tunnel FET or a transistor structure using a ferroelectric material with negative capacitance (NC) effect was studied [10–12]. It is known that the NC FETs have more advantages in on-current than tunnel FETs [13]. NC FETs with ferroelectric materials not only reduce the subthreshold swing dramatically due to the negative capacitance effect, while also increasing on-current with reducing off-current, but also have the advantages of low leakage current and high frequency operation [14–16]. However, the threshold voltage is changed due to the use of ferroelectric material, which has an effect on drain induced barrier lowering (DIBL) [17]. In this paper, the change of the DIBL in negative capacitance FET using ferroelectric material is to be investigated. It is known that the DIBL has a positive value in a 3D FET, but shows a negative value in NC FETs as it changes according to the ferroelectric thickness [18]. The fact that the DIBL is negative means that the threshold voltage increases as the drain voltage increases. Therefore, we intend to analyze the DIBL of NC FET by observing this phenomenon in detail in this paper. The analytical model of DIBL will be presented in order to analyze this. In addition, after finding the relationship between the drain current and the gate voltage below the threshold voltage using the two-dimensional potential distribution model, the threshold voltage derived from the second derivative method [19] will be compared with the result of this analytical model.

A junctionless double-gate (JLDG) FET was used for the transistor structure with a ferroelectric material. The junctionless FET is easy to process because it does not need to form an abrupt junction between source/drain and channel when scaled-down, and it has the characteristics of showing superior threshold voltage and subthreshold swing immunity to hot carrier degradation than conventional FETs [20]. In the case of a conventional FET, most of the current flows to the insulator/semiconductor interface, but in the case of a junctionless FET, the center of the channel has a lower potential than the interface, so most of the current flows to the central channel [21,22]. Therefore, the threshold voltage will be directly affected by the change of the central potential [23–25]. Based on the same basic theory, an analytical model of DIBL was derived using change of the central potential. In particular, a metal-ferroelectric-metal-insulator-semiconductor (MFMIS) structure was used for the gate structure, and hafnium zirconium oxide (HZO) was used as the ferroelectric material. This structure is known to be more stable as a structure in which the negative capacitance caused by ferroelectric and the metal-insulator-semiconductor capacitance are connected in series [26].

Rassekh et al. calculated the DIBL of a negative capacitance FET using parabolic potential distribution, but this model has a drawback in that it is not possible to obtain an accurate potential distribution from the surface and the center at the same time when the channel length is 30 nm or less [27,28]. Awadhiya et al. analyzed the threshold voltage and DIBL when MFMIS was used for the gate structure of a conventional FET [29]. Saha et al. described a negative DIBL using a metal-ferroelectric-insulator-semiconductor (MFIS) gate structure [30]. Therefore, in this paper, when the gate structure of the JLDG FET is an MFMIS structure, an analytical model of DIBL will be presented using the potential distribution in the current path, and a comparative analysis will be conducted with the DIBL derived from a two-dimensional potential distribution.

2. DIBL of ferroelectric NC FET

2.1. Structure of ferroelectric NC FET

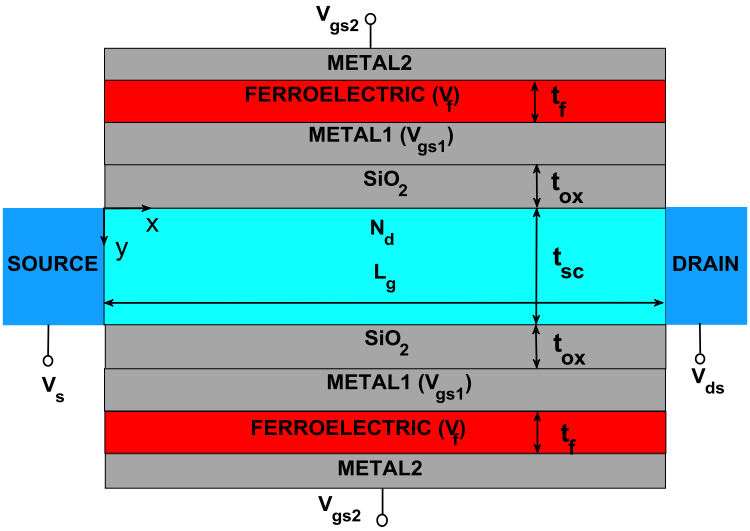

Figure 1. Schematic diagram of a symmetric junctionless double-gate FET with ferroelec -tric material as the stacked gate oxides.

Figure 1 shows the cross-sectional view of the NC FET with the MFMIS structure used in this paper. The source/drain and channel were equally highly doped with N_d^+, and a symmetrical JLDG FET with the same top and bottom gates was used. In this paper, $N_d^+ = 10^{19}/\text{cm}^3$ was used. The voltage applied to the outer metal is V_{gs2}, the voltage induced to the inner metal is V_{gs1}, and the voltage of the ferroelectric material is V_f. Table 1 shows the device parameters used in this paper. Quantum-mechanical analysis with tunneling current is required when the channel length is less than 10 nm, but this effect was not included in this paper because DIBL was observed only for transistors with a channel length of 20 nm or more [31].

Table 1. Device parameters for this analytical threshold voltage model.

Device parameter	Symbol	Value
Channel length	L_g	20-60 nm
Channel width	W	1 μm
Channel thickness	t_{sc}	5-10 nm
SiO_2 thickness	t_{ox}	1-4 nm
Doping concentration	N_d	10^{19} /cm^3
Ferroelectric thickness	t_f	0-10 nm
Remanent polarization	P_r	17 μC/cm^2
Coercive field	E_c	1.2 MV/cm

2.2. Analytical DIBL model of NC FET

Using the potential model of Ding et al. such as Eq (1) and the definition of threshold voltage

and DIBL, the analytical model of the DIBL can be obtained [31].

$$\varphi(x,y) = V_s + \frac{V_{ds}}{L_g}x + \sum_{n=1}^{\infty}\left[C_n e^{k_n y} + D_n e^{-k_n y} - f_n / k_n^2\right]\sin\frac{n\pi x}{L_g} \tag{1}$$

where V_s and V_{ds} are the source and drain voltages, respectively, and C_{ox} is the capacitance of SiO_2. The C_n, D_n, k_n, f_n, etc. are mentioned in the reference [32]. At this time, the potential distribution at the center point $y = t_{sc}/2$ through which most of the current flows due to the characteristics of the JLDG MOSFET is calculated, and the potential value at the lowest point $x = x_{min}$ of the potential distribution is calculated as the followings.

$$\varphi(x_{\min},\frac{t_{sc}}{2}) = V_s + \frac{V_{ds}}{L_g}x_{\min} + \sum_{n=1}^{\infty}\left[2C_n e^{k_n t_{sc}/2} - f_n / k_n^2\right]\sin\left(\frac{n\pi x_{\min}}{2}\right) \tag{2}$$

If the inner gate voltage to satisfy Eq (3) is obtained, the threshold voltage V_{th1} of inner metal can be obtained.

$$\varphi(x_{\min},\frac{t_{sc}}{2}) = 0 \tag{3}$$

At this time, using the voltage V_f and charge Q in the ferroelectric, the voltage applied to the outer metal can be obtained as follows [33].

$$V_{gs2} = V_f + V_{th1} \tag{4}$$

$$V_f = 2\alpha t_f Q + 4\beta t_f Q^3 + 6\gamma t_f Q^5 \tag{5}$$

Therefore, the threshold voltage is

$$V_{th} = 2\alpha t_f Q + 4\beta t_f Q^3 + 6\gamma t_f Q^5 + V_{th1} \tag{6}$$

The α, β, γ are obtained from the *P-E* hysteresis curve between the ferroelectric polarization *P* and the electric field *E* extracted from the ferroelectric capacitor. That is, using the remanent polarization P_r and coercive field E_c in the *P-E* hysteresis curve, it can be obtained as follows [34].

$$\begin{aligned}\alpha &= -\frac{3\sqrt{3}}{2}\frac{E_c}{P_r}\\ \beta &= \frac{3\sqrt{3}}{2}\frac{E_c}{P_r^3}\end{aligned} \tag{7}$$

In this paper, $P_r = 17\,\mu C/cm^2$ and $E_c = 1.2\,MV/cm$ as experimental results of HZO film were used to find the α, β, and $\gamma = 0$ [29].

In Eq (6), Q is the charge of the ferroelectric material in the subthreshold, which can be obtained as follows using the method of the reference [27,35].

$$Q = C_{ox}\left[(V_{gs1} - \Delta\varphi_{ms} - \frac{V_{ds}}{2}) + \sum_{n=1}^{\infty}\left[2C_n e^{k_n t_{sc}/2} - f_n / k_n^2\right]\left(\frac{1}{n\pi}\right)\left[(-1)^n - 1\right]\right] \tag{8}$$

where $\Delta\varphi_{ms}$ is the work function difference between metal and semiconductor.
According to the definition of DIBL,

$$DIBL = -\frac{\Delta V_{th2}}{\Delta V_{ds}} = -\frac{\Delta V_f}{\Delta V_{ds}} - \frac{\Delta V_{th1}}{\Delta V_{ds}} \approx -2\alpha t_f \frac{\Delta Q}{\Delta V_{ds}} - 4\beta t_f\left[\Delta Q^3 + 3Q_{low}Q_{high}\Delta Q\right] - \frac{\Delta V_{th1}}{\Delta V_{ds}} \tag{9}$$
$$\Delta Q = Q_{high} - Q_{low}$$

Here, Q_{low} and Q_{high} are ferroelectric charges at low and high drain voltages, respectively, and it can be ignored because the second term on the right side of Eq (9) is very small. That is to say, the DIBL can be expressed as

$$DIBL \approx -2\alpha t_f \frac{\Delta Q}{\Delta V_{ds}} - \frac{\Delta V_{th1}}{\Delta V_{ds}}\bigg|_{t_f=0} \tag{10}$$

In Eq (10), since α is negative and $\Delta Q / \Delta V_{ds}$ is also negative, it will eventually be smaller than $-\Delta V_{th1} / \Delta V_{ds}$, which is a positive value of DIBL when t_f = 0.

To examine this in detail, Figure 2 shows the relationship between the voltage across the ferroelectric and the ferroelectric charge with respect to the change in the drain voltage. As can be seen from Figure 2(a), $-\Delta V_f / \Delta V_{ds}$ is a negative number. Therefore, as described above, the DIBL of the NC FET with ferroelectric material will be smaller than $-\Delta V_{th1} / \Delta V_{ds}$, the DIBL when t_f = 0 nm. In particular, since the value $\Delta V_f / \Delta V_{ds}$ increases as the channel length decreases, the DIBL of the NC FET will further decrease when the channel length decreases. Also, as t_f increases, so $\Delta V_f / \Delta V_{ds}$ also increases. Therefore, the reduction effect of DIBL will increase with the increase of t_f. This effect is eventually caused by the change according to the drain voltage of the charge in ferroelectric. As can be seen from Figure 2(b), the DIBL of NC FET will decrease because $\Delta Q / \Delta V_{ds}$ is negative.

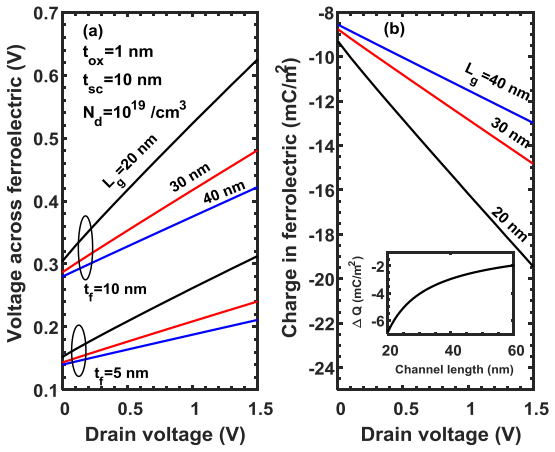

Figure 2. (a) Voltage across ferroelectric for drain voltage with the channel length and ferroelectric thickness as parameters and (b) the charge in ferroelectric with the channel length as a parameter.

At this time, the absolute value of ΔQ increases in the inset of Figure 2(b) as the channel length decreases, so it can be seen that the DIBL of the NC FET will further decrease with the decrease of the channel length. Ferroelectric materials can be used in this way to reduce the DIBL.

In order to examine this effect in detail, Figure 3(a) shows the drain current-gate voltage induced using Eq (11) with the potential distribution of Eq (1). The validity of Eq (11) has been mentioned in the previous paper [36].

$$I_d = \frac{qn_i\mu_n WkT\left\{1-\exp\left(\frac{-qV_{ds}}{kT}\right)\right\}}{\int_0^{L_g}\frac{1}{\int_0^{t_{sc}}\exp\left(\frac{q\phi(x,y)}{kT}\right)dy}dx} \tag{11}$$

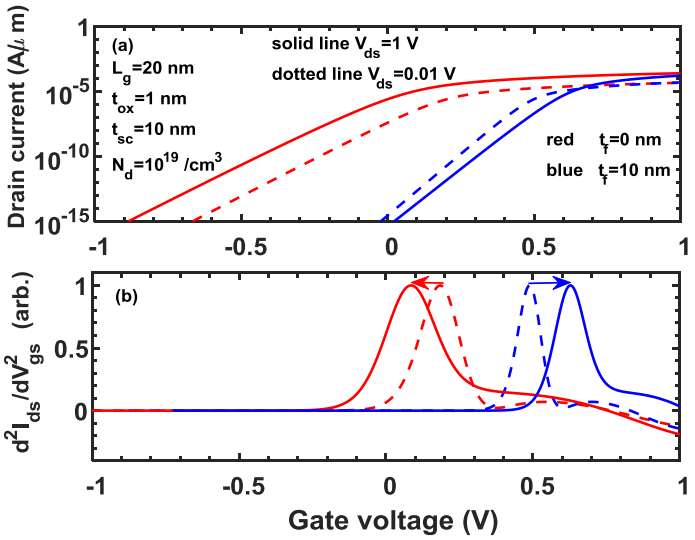

Figure 3. (a) Curves of drain current vs. gate voltage for t_f = 0 nm and t_f = 10 nm at V_{ds} = 1 V (high) and V_{ds} = 0.01 V (low) and (b) second derivative of curves of drain current vs. gate voltage to obtain the threshold voltage. Threshold voltage is indicated by the peaks on the curve.

Figure 3(a) shows the relationship between drain current and gate voltage when the ferroelectric thickness is 0 nm and 10 nm. In Figure 3(b), the threshold voltage was obtained by the second derivative method. As a result, it can be seen that the DIBL is generally positive when t_f = 0 nm. That is, it can be observed that the threshold voltage decreases as V_{ds} increases. However, it can be seen that the threshold voltage increases if V_{ds} increases when t_f = 10 nm, and the DIBL becomes negative. Note that this is consistent with the description in Eq (10).

The negative DIBL can also be observed in the central potential distribution. That is, the central potential distribution is shown when the drain voltage is 1 V and 0.01 V under the conditions given in Figure 4. As can be seen from Figure 4, it can be seen that the minimum potential value is lower when V_{ds} = 1 V than when V_{ds} = 0.01 V. This indicates that the threshold voltage increases when V_{ds} = 1 V from the threshold voltage definition in Eq (3), so that the DIBL can have a negative value according to the definition. Since the degree of the negative DIBL varies with the channel size and ferroelectric thickness of JLDG FET, this will be considered in detail.

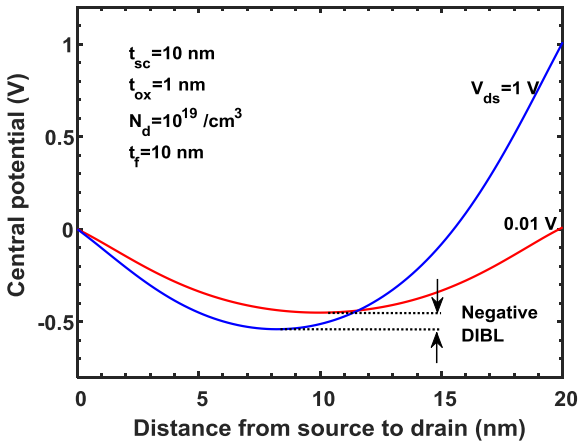

Figure 4. Central potential distributions for V_{ds} = 0.01 V and V_{ds} = 1 V for the channel length of 20 nm.

3. Results

3.1. Validity of this DIBL model

In order to verify the validity of Eq (10), the results of other papers and TCAD and the DIBL obtained using the method of Figure 3 described above were compared in Figure 5. As shown in Figure 5, the DIBL obtained using the model of Eq (10) agrees well with the DIBL obtained using the second derivative method of the I_d-V_{gs} curve. Also, it was in good agreement with the results of TCAD for t_f = 0. As mentioned in reference [28], the results of TCAD are shown using ΔV_T and $\Delta\phi_{min}$. As a result of comparison with the Rassekh model, the shorter the channel length, the greater the difference with the results of this paper. This is because the Rassekh model uses a parabolic potential distribution and the accuracy is lowered when the channel length is smaller than 30 nm as described above. The DIBL decreases when t_f = 5 nm and t_f = 10 nm where the ferroelectric is present than when t_f = 0 nm (conventional JLDG FET). The DIBL is decreased in the case of NC FET because the effect of $-\Delta V_f / \Delta V_{ds}$ is added to $-\Delta V_{th1} / \Delta V_{ds}$ that is the DIBL at t_f = 0 nm.

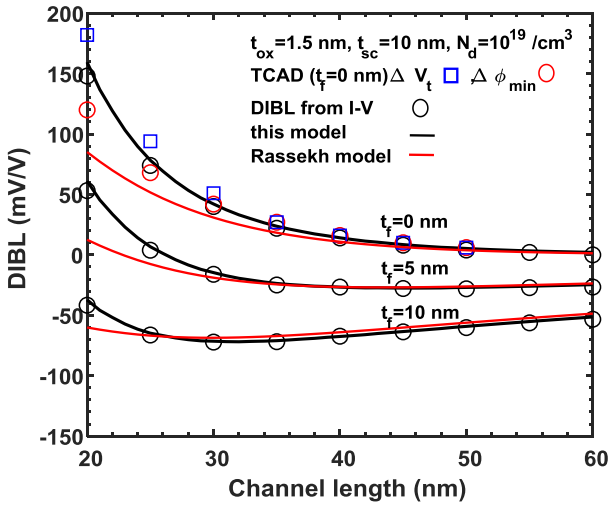

Figure 5. Comparisons of DIBLs of Eq (10) with results of other papers and TCAD.

3.2. Analysis of DIBL for JLDG MOSFET with ferroelectric

The ferroelectric thickness of NC FETs will have the greatest influence on the DIBL. First, the contour of the DIBL in the range of ferroelectric thickness of 0~10 nm and channel length of 20~60 nm is shown in Figure 6. As can be seen from Figure 6, as the ferroelectric thickness increased, the negative DIBL characteristics were shown, and as the channel length increased, the critical ferroelectric thickness showing negative DIBL characteristics was decreasing. In addition, as the ferroelectric thickness decreased, the change in DIBL according to the channel length was very severe, and the negative DIBL characteristics were always shown at the channel length of 20 nm ≤ L_g ≤ 60 nm when the ferroelectric thickness was increased to 8 nm under the given conditions.

As shown in Figure 6, the sign of DIBL is changing starting from the line DIBL = 0 mV/V. In order to investigate the tendency of DIBL sign conversion, the contour line of DIBL = 0 mV/V is shown in Figure 7(a) using the thickness of the insulator layer, SiO_2, as a parameter.

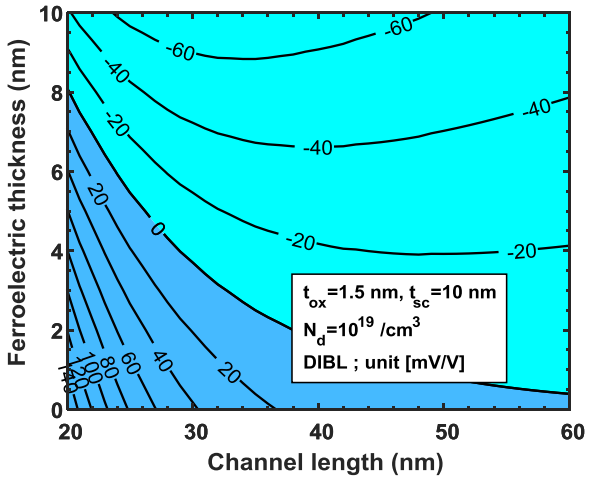

Figure 6. Contours of DIBL for the ferroelectric thickness and channel length under the given conditions.

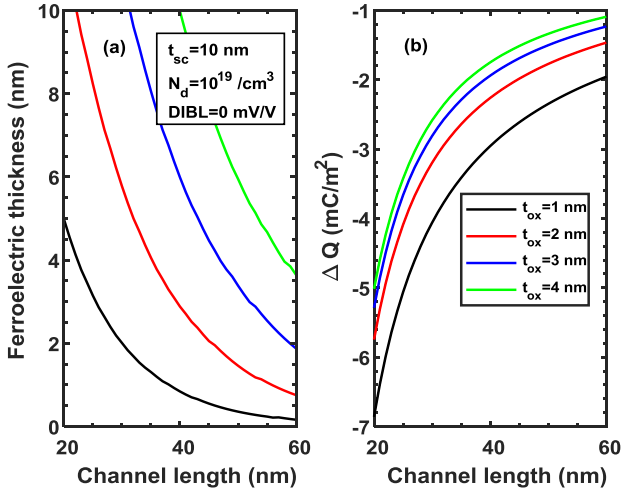

Figure 7. (a) Contours of DIBL = 0 mV/V for the ferroelectric thickness and channel length and (b) difference of the charge in ferroelectric at high and low drain voltage with the oxide thickness as a parameter.

As can be seen from Figure 6, the upper part of the contours of Figure 7(a) is the area where DIBL is negative. Observing Figure 7(a), it can be seen that the area in which DIBL is negative decreases as the thickness of SiO_2 used as an oxide film increases. That is, if the thickness of SiO_2 increases at the same channel length, the ferroelectric thickness must also increase in order to exhibit the negative DIBL characteristics. In particular, it can be observed that the ferroelectric thickness should increase significantly when the thickness of SiO_2 increases in the range of small channel length. This phenomenon is ultimately due to the change of ΔQ according to the thickness of SiO_2 in Eq (10). Figure 7(b) shows the change in ΔQ according to the channel length with the thickness of SiO_2 as a parameter. As can be seen from Figure 7(b), it can be observed that the absolute value of ΔQ decreased as the thickness of SiO_2 increases. As a result, it can be seen that the absolute value of the first term on the right side of Eq (10) decreases with the increase of the thickness of SiO_2, and the DIBL increases as the thickness of SiO_2 increases. Therefore, as the thickness of SiO_2 increases in Figure 7(a), the negative area of the DIBL decreases. In addition, it can be seen that the DIBL = 0 mV/V contour interval becomes wider for smaller channel length because the variability of ΔQ for the thickness of SiO_2 increases as the channel length decreases.

An important factor in determining the characteristics of a transistor is its silicon thickness. Figure 8(a) shows the contours of DIBL = 0 mV/V for channel length and ferroelectric thickness with silicon thickness as a parameter.

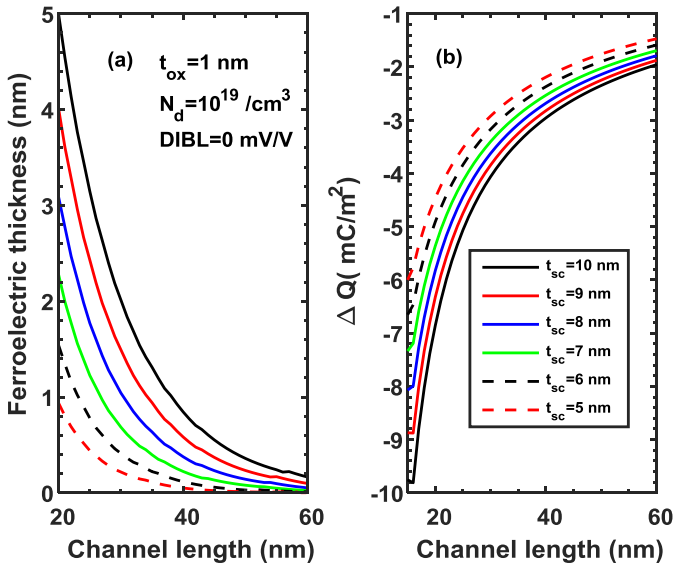

Figure 8. Contours of DIBL = 0 mV/V for the ferroelectric thickness and channel length with the silicon thickness as a parameter.

As shown in Figure 8, if the silicon thickness decreases, a region with DIBL < 0 mV/V occurs even when the ferroelectric thickness is small. This is because the DIBL at t_f = 0 is very small when silicon thickness is small, so even if ΔQ is small, it easily enters the region where DIBL < 0 mV/V. As t_{sc} increases, the DIBL at t_f = 0 also increases. Therefore, it can be observed that even if the absolute value of ΔQ increases, a relatively thick ferroelectric thickness is required for DIBL to become negative, and the region with DIBL < 0 mV/V is decreasing. As can be seen from Figure 8, the influence of DIBL by t_{sc} becomes very large when the channel length is shortened to about 20 nm, but it easily enters the DIBL < 0 mV/V region regardless of silicon thickness or ferroelectric thickness when the channel length is increased to about 60 nm.

4. Conclusions

The DIBL of JLDG MOSFET using ferroelectric material was analyzed in this paper. In the case of these NC FETs, it was found that the DIBL had a negative value according to the ferroelectric thickness, and the cause was analyzed. Fundamentally, the threshold voltage rises when the drain voltage increases due to the properties of the ferroelectric material. This fact was confirmed from the drain current-gate voltage relationship with the change in the central potential. An analytical DIBL model was presented for the analysis, and it was confirmed that it was in good agreement with the DIBL obtained from the drain current-gate voltage relationship induced using the two-dimensional potential distribution. Of course, a comparison with TCAD and other papers confirmed the validity of this model. The negative DIBL was eventually observed because the change of charge in ferroelectric with respect to the change in drain voltage affects the voltage across ferroelectric. It was observed that the DIBL tends to become negative as the ferroelectric thickness increases when the channel length is the same. In the analysis according to t_{ox}, the thickness of SiO_2 used as an insulator in the MFMIS structure and silicon thickness t_{sc}, it was observed that the negative DIBL phenomenon easily appeared as the t_{ox} and t_{sc} decreased.

Conflict of interest

All authors declare no conflicts of interest in this paper.

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