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Research article

Analytical models of threshold voltage and drain induced barrier lowering in junctionless cylindrical surrounding gate (JLCSG) MOSFET using stacked high-*k* oxide

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Abstract: We proposed the analytical models to analyze shifts in threshold voltage and drain induce d barrier lowering (DIBL) when the stacked SiO_2/high-*k* dielectric was used as the oxide film of Junc tionless Cylindrical Surrounding Gate (JLCSG) MOSFET. As a result of comparing the results of the presented model with those of TCAD, it was a good fit, thus proving the validity of the presented m odel. It could be found that the threshold voltage increased, but DIBL decreased by these models as t he high-*k* dielectric constant increased. However, the shifts of threshold voltage and DIBL significant ly decreased as the high-*k* dielectric constant increased. As for the degree of reduction, the channel le ngth had a greater effect than the thickness of the high-*k* dielectric, and the shifts of threshold voltage and DIBL were kept almost constant when the high-*k* dielectric constant was 20 or higher. Therefor e, the use of dielectrics such as HfO_2/ZrO_2, La_2O_3, and TiO_2 with a dielectric constant of 20 or more f or stacked oxide will be advantageous in reducing the short channel effect. In conclusion, these mode ls were able to sufficiently analyze the threshold voltage and DIBL.

Keywords: cylindrical surrounding gate; junctionless; threshold voltage; DIBL; stacked oxide; high-*k*

1. Introduction

As the channel length of the transistor decreases to sub-10 nm or less, the conventional transistor structure becomes increasingly difficult to use due to the short channel effects [1–3]. For

high-speed operation, low power consumption, and improved productivity, the reduction of transistor size is becoming the greatest competitiveness of all integrated circuit manufacturers. Transistors of various structures have been developed and used to reduce the short channel effects that inevitably occurs due to the reduction in transistor size. In particular, FinFET is widely used in Qualcomm's communication chips. FinFET has a tri-gate structure and it has been shown to have excellent control of carriers in the channel even at channel length and fin width of sub-10 nm [4,5]. In order to improve the gate control capability, the four-gate structure called Omega-FET, was developed [6]. Omega-FET is a structure in which the gate is wrapped around a rectangular channel, so that the control capability by the gate terminal is improved than that of FinFET. However, the Omega-FET has a problem of the corner-effect that inevitably occurs in the square structure. The structure developed to solve this problem is a cylindrical surrounding gate (CSG) MOSFET. The CSG MOSFET has been developed to cope with the short channel effects more than the FinFET used in various application ranges [7,8]. The CSG MOSFET is a structure in which the gate terminal completely encloses the cylindrical channel. As it is known as the most effective structure for controlling the carriers in the channel by the gate terminal as well as removing the corner effect that occurs in the Omega-FET, many studies are being conducted [9,10].

As the channel length is shortened, not only the structural problem of the channel but also the doping technology are causing problems. In the junction-based 3D FET of the inversion type using the PN junction formed between the source/drain and the channel, the reduction of channel length makes the PN junction process difficult, and the channel formation difficult due to the depletion layer effect that occurs in the PN junction. The MOSFET developed to solve this problem is the junctionless MOSFET [11,12]. A lot of research has been carried out since this structure was presented by Colinge et al., and it is a structure that can solve the difficulty of the process because it is not necessary to form a PN junction between the cannel and source/drain region [13]. In particular, in many studies, it has been known that the short-channel effects are more significantly reduced in the accumulation type which is a junctionless MOSFET than in the inversion type MOSFET that is a junction-based MOSFET [14,15].

In addition to the above problems, there are many problems in the thickness of the gate oxide layer with the reduction of the channel length due to scaling effects. According to the scaling rule, the thickness of the gate oxide film must be reduced in proportion to the channel length. However, when the thickness of the gate oxide is decreased, not only a problem in the process but also another short channel effects occurs due to an increase in gate parasitic current. As the reduction of the gate oxide film hits its limit, many efforts are made to use a high-k oxide film as the gate oxide film to reduce the short channel effects and gate leakage current [16–22]. However, the high-k oxide film material has a limitation in reducing the gate parasitic current due to a small band offset, generating roughness of the interface with silicon used as a channel. A structure that has emerged to solve this problem is a stacked structure of a gate oxide film. In this structure, SiO_2 is used for the part in contact with the silicon channel and the high-k dielectric is used for the part in contact with the gate metal, thereby solving the short channel effect caused by the reduction of the gate oxide thickness. Rasol et al. analyzed the I_{off} current for a junctionless cylindrical surrounding gate(JLCSG) MOSFET using stacked high-k oxide by ATLAS, and Darwin et al. used HfO_2, $HfSiO_4$, Al_2O_3, Si_3N_4, etc. as high-k materials, but the short-channel effects of the junctionless cylindrical MOSFET was analyzed using only the parametric form of the potential distribution [23,24]. Also Kosmani et al. analyzed the short-channel effects by TCAD, using a high-k oxide film in a junction-based double

gate and Gate-All-Around MOSFET [25]. S. Gupta et al. obtained the potential distribution of the dual gate metal junctionless cylindrical gate-all-around (JLC-GAA) MOSFET, using HfO_2 as a high-k material [26]. As such, many researchers are trying to reduce the short channel effect of JLCSG MOSFETs by using stacked high-k materials. In this study, in order to meet this purpose, the analytical threshold voltage and DIBL model were proposed using the definition of the threshold voltage and DIBL which are a kind of the short channel effects. We will prove the validity of the proposed models and analyze the threshold voltage and DIBL using the proposed models to consider the phenomenon of short-channel effects reduction in the case of using SiO_2/high-k gate oxide stacked on the JLCSG MOSFET. As a high-k dielectrics, we will use SiO_2 ($\varepsilon_s = 3.9$), Al_2O_3 ($\varepsilon_s = 9$), Y_2O ($\varepsilon_s = 15$), HfO_2/ZrO_2 ($\varepsilon_s = 25$), La_2O_3 ($\varepsilon_s = 30$), TiO_2 ($\varepsilon_s = 80$).

2. Threshold voltage and DIBL models for JLCSG MOSFET

2.1. Potential distributions in the channel of JLCSG MOSFET

Figure 1 shows the schematic diagram of the JLCSG MOSFET used in this paper. The source, drain, and channel were doped with n-type of high concentration, and a metal with a work function of ϕ_m was used. L_g denotes the length of the channel, R the radius of the silicon. The t_{SiO2} is the thickness of the SiO_2 oxide layer bonded to the silicon channel, and the t_{hk} the thickness of the high-k material, which is in contact with the gate metal, and these two dielectrics are stacked. The t_{SiO2} used 1 nm, and the t_{hk} between 1 nm and 5 nm in this paper. The V_{gs}, V_{ds}, and V_s represent a gate voltage, a drain voltage, and a source voltage, respectively. At this time, the potential distribution of the JLCSG MOSFET was obtained using the following Poisson equation [24,26,27].

$$\frac{1}{r}\frac{\partial}{\partial r}\left[r\frac{\partial}{\partial r}\phi(r,z)\right]+\frac{\partial^2\phi(r,z)}{\partial z^2}=-\frac{qN_d}{\varepsilon_{si}} \tag{2.1}$$

Here, ε_{si} is the dielectric constant of silicon, and N_d is 10^{19} /cm^3 as the channel doping concentration. Using the superposition technique, the potential distributions in channel region are expressed as follows.

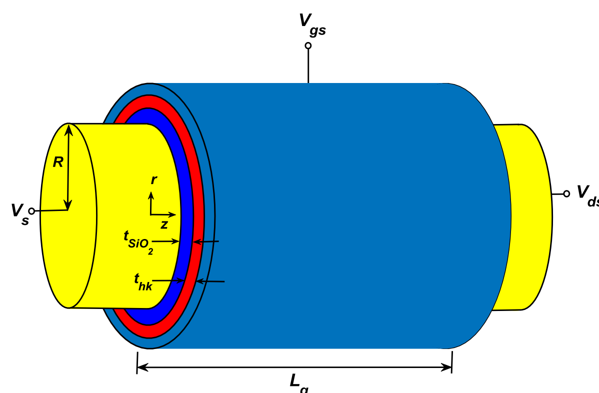

Figure 1. Schematic cross-sectional diagram of the cylindrical surrounding gate (CSG) MOSFET.

$$\phi(r,z)=\phi_1(r)+\phi_2(r,z) \tag{2.2}$$

Here, $\phi_1(r)$ is the one dimensional solution to Poisson's equation and $\phi_2(r, z)$ is the two dimensional solution to the homogenous Laplace equation, which is expressed as follows.

$$\frac{1}{r}\frac{\partial}{\partial r}\left(r\frac{\partial\phi_1(r)}{\partial r}\right)=-\frac{qN_d}{\varepsilon_{si}} \tag{2.3}$$

$$\frac{\partial^2\phi_2(r,z)}{\partial r^2}+\frac{1}{r}\frac{\partial\phi_2(r,z)}{\partial r}+\frac{\partial^2\phi_2(r,z)}{\partial z}=0 \tag{2.4}$$

To solve (2.3), the following boundary conditions are used [28].

$$\begin{aligned}\left.\frac{\partial\phi_1(r)}{\partial r}\right|_{r=0}&=0\\ \left.\frac{\partial\phi_1(r)}{\partial r}\right|_{r=R}&=\frac{C_{ox}}{\varepsilon_{si}}\left[V_{gs}-\phi_{ms}-\phi_1(R)\right]\end{aligned} \tag{2.5}$$

where V_{gs} is the applied voltage of the gate and ϕ_{ms} is the work function difference between gate metal and silicon. The C_{ox} is expressed as follows [29].

$$\begin{aligned}C_{ox}&=\frac{\varepsilon_{SiO_2}}{R\ln(1+t_{oxeff}/R)}\\ t_{oxeff}&=t_{SiO_2}+(\varepsilon_{SiO_2}/\varepsilon_{hk})t_{hk}\end{aligned} \tag{2.6}$$

At this time, the solution to (2.3) is as follows [30].

$$\phi_1(r)=-\frac{qN_d}{4\varepsilon_{si}}r^2+V_{gs}-\phi_{ms}+\frac{qN_dR}{2C_{ox}}+\frac{qN_dR^2}{4\varepsilon_{si}} \tag{2.7}$$

Since the method of calculating $\phi_2(r,z)$ from (2.4) is independent of the doping distribution, using the variable separation method and Fourier-Bessel series by the method of C. Li et al. [30], $\phi_2(r,z)$ is as follows.

$$\phi_2(r,z)=\sum_{n=1}^{\infty}\left[C_n\exp\left(\frac{\alpha_n z}{R}\right)+D_n\exp\left(-\frac{\alpha_n z}{R}\right)\right]J_0\left(\frac{\alpha_n r}{R}\right) \tag{2.8}$$

where α_n is eigenvalue that satisfy the following equation.

$$RJ_0(\alpha_n) - \frac{\varepsilon_{si}}{C_{ox}} \alpha_n J_1(\alpha_n) = 0 \tag{2.9}$$

In (2.8), C_n and D_n are obtained using the following boundary conditions [28].

$$\begin{aligned} &\phi(r, z = 0) = V_F \\ &\phi(r, z = L) = V_F + V_{ds} \\ &V_F = \frac{kT}{q} \ln\left(\frac{N_d}{n_i}\right) \end{aligned} \tag{2.10}$$

At this time, because the first term dominates the series of (2.8) due to rapid decay of the Fourier-Bessel series, only C_1 and D_1 were used as follows.

$$\begin{aligned} C_1 &= \frac{A\left[\exp(-\lambda_1) - 1\right] - B}{2\sinh(-\lambda_1)} \\ D_1 &= \frac{A\left[1 - \exp(\lambda_1)\right] + B}{2\sinh(-\lambda_1)} \\ \lambda_1 &= \frac{\alpha_1 L}{R} \\ A &= \frac{-2}{J_0^2(\alpha_1) + J_1^2(\alpha_1)} \frac{J_1(\alpha_1)}{\alpha_1} \left(V_{gs} - \phi_{ms} + \frac{qN_D R}{2C_{ox}} + \frac{qN_D R^2}{4\varepsilon_{si}} - V_F \right) \\ &\quad + \frac{qN_D}{2\varepsilon_{si}} \frac{1}{J_0^2(\alpha_1) + J_1^2(\alpha_1)} \frac{\alpha_1 J_1(\alpha_1) - 2J_2(\alpha_1)}{(\alpha_1 / R)^2} \\ B &= \frac{2V_{ds}}{J_0^2(\alpha_1) + J_1^2(\alpha_1)} \frac{J_1(\alpha_1)}{\alpha_1} \end{aligned} \tag{2.11}$$

Substituting (2.7), (2.8), and (2.11) into (2.2), the potential distribution of the JLCSG MOSFET in the channel can be obtained.

2.2. The threshold voltage and DIBL of JLCSG MOSFET

The analytical threshold voltage model is derived using the definition of the threshold voltage and the distribution of electrostatic potential in the previous section. The junctionless MOSFET operates in accumulation mode, and the gate voltage is defined as the threshold voltage when the minimum value of the central potential distribution becomes V_F [31]. In other words, the gate voltage that satisfies

$$\phi_{\min} = \phi(0, z_{\min}) = V_F \tag{2.12}$$

must be obtained. At this time, $z_{\min}$ represents the z value at which the central potential distribution becomes the minimum, and is given as [28].

$$z_{\min} = \left(\frac{R}{2\alpha_1}\right)\ln\left(\frac{D_1}{C_1}\right) \tag{2.13}$$

S. K. Gupta et al. obtained the threshold voltage by the same method, but ignored the dependence of V_{gs} to the variables A, B, and $z_{\min}$ [32]. Therefore, in this paper, the following threshold voltage V_{th} can be obtained as in Appendix A if V_{gs} that satisfies (2.12) is obtained.

$$V_{th} = \frac{1}{2\left[a_1/\sinh^2(-\lambda_1)-1\right]}\left\{-\left[a_2/\sinh^2(-\lambda_1)-2H\right]+\sqrt{\left[a_2/\sinh^2(-\lambda_1)-2H\right]^2 - 4\left[a_1/\sinh^2(-\lambda_1)-1\right]\left[a_3/\sinh^2(-\lambda_1)-I\right.} \right. \tag{2.14}$$

The constants a_1, a_2, a_3 and H are indicated in Appendix A. In order to prove the validity of (2.14), it was compared in Figure 2 with Hu's model [28].

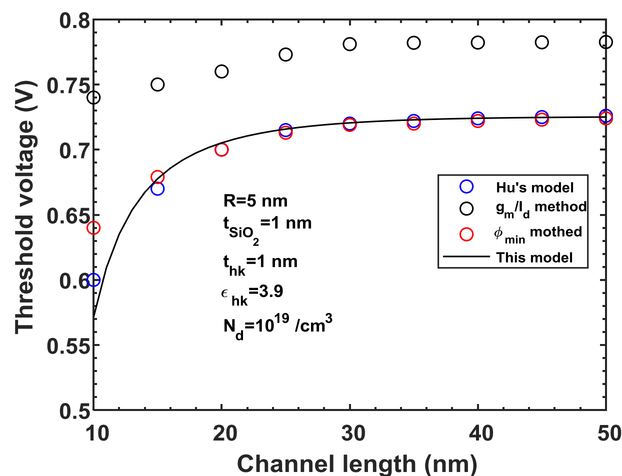

Figure 2. Comparisons of the various threshold voltages with this model (2.14).

As seen in Figure 2, the threshold voltage obtained by the g_m/I_d method is overestimated. It can be seen that (2.14) suggested in this paper agrees well with Hu's model. However, it can be found that a difference between the threshold voltages occurs when the channel length is reduced to 10 nm.

The DIBL is a measure of the change of the threshold voltage to the drain voltage. In the previous paper [33–35], the change of the threshold voltage was calculated when the drain voltages are changed from $V_{ds} = 0.1$ V to $V_{ds} = 0.5$ V or 1.0 V to obtain the DIBL. However, in this paper, using the definition of the DIBL and (2.14), the following DIBL could be obtained through the same process as in Appendix B.

$$DIBL = -\frac{1}{2\left[a_1 - \sinh^2(\lambda_1)\right]}\left\{\frac{\begin{matrix} X^2\left(\exp(-\lambda_1)+\exp(\lambda_1)-2\right)+ \\ \left\{\begin{matrix}\left(\frac{a_2}{\sinh^2(\lambda_1)}-2H\right)\left(-X^2\left(\exp(-\lambda_1)+\exp(\lambda_1)-2\right)\right)- \\ 2\left(\frac{a_1}{\sinh^2(\lambda_1)}-1\right)\left(-XY\left(\exp(-\lambda_1)+\exp(\lambda_1)-2\right)-2X^2V_{ds}\right)\end{matrix}\right\}\end{matrix}}{\sqrt{\left[a_2/\sinh^2(\lambda_1)-2H\right]^2-4\left[a_1/\sinh^2(\lambda_1)-1\right]\left[a_3/\sinh^2(\lambda_1)-H^2\right]}}\right\} \quad (2.15)$$

In (2.15), X and Y values are indicated in Appendix A. It can be shown in (2.15) that the DIBL changes according to the value of V_{ds}. That is, the DIBL value changes according to the V_{ds} value measuring DIBL. In order to prove the validity of (2.15), the DIBL values of other models in Figure 3 were compared under the same conditions. As a result, it can be observed that it fits well with the results of other models. However, it can be observed that the errors between models increase as the channel length decreases. As above, since the validity of the threshold voltage model (2.14) and DIBL model (2.15) presented in this paper has been verified, we will use these equations to observe the characteristics of the JLCSG MOSFET with the stacked oxide film of SiO_2 and high-*k* dielectrics. Device parameters used in this study are listed in Table 1.

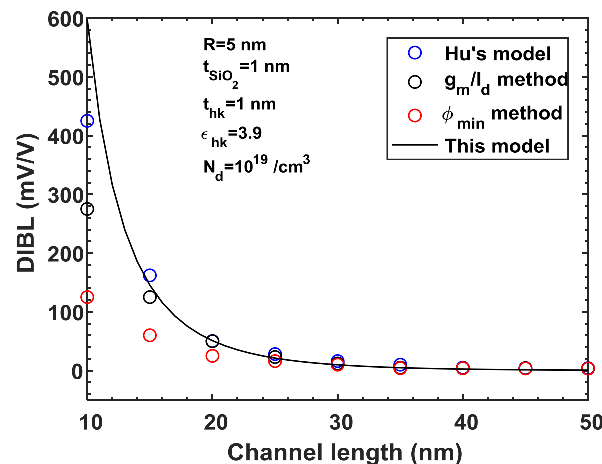

Figure 3. Comparison of the various DIBLs with this model (2.15).

Table 1. Device parameters used in these models.

Device parameter	Symbol	Value
Channel length	L_g	10 - 30 nm
Silicon radius	R	5 nm
Doping concentration	N_d	10^{19} /cm^3
Thickness of SiO_2	t_{SiO2}	1 nm
Thickness of high-k dielectric	t_{hk}	1 - 5 nm
Permittivity of high-	ε_{hk}	3.9 - 80

3. Analysis of threshold voltage and DIBL for JLCSG MOSFET by these models

In the structure of Figure 1, the change of the threshold voltage with respect to the dielectric constant of the high-*k* material is calculated with the drain voltage as a parameter as shown in Figure 4. The difference in threshold voltage is indicated by arrows in Figure 4 when the drain voltage increases from 0.1 V to 1.1 V for a specific high-*k* material. As shown in Figure 4, as the dielectric constant of high-*k* material increases, the threshold voltage increases, but the threshold voltage is almost constant from the dielectric constant of 20. As shown in Figure 4, DIBL, which is the difference between the threshold voltage at the drain voltage of 0.1 V and the threshold voltage at 1.1 V, shows a larger value as the dielectric constant decreases, but gradually decreases as the dielectric constant of high-*k* increases. Therefore, the value is an almost constant at the dielectric constant of high-*k* of above 20.

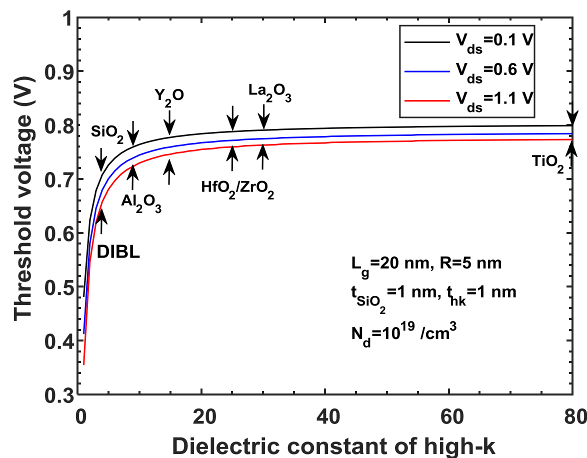

Figure 4. Threshold voltages for dielectric constant of high-*k* with the drain voltage as a parameter

Figure 5 shows the change of the DIBL calculated using (2.15) according to the high-*k* permittivity. As seen in Figure 5, the DIBL appears large when the high-*k* dielectric constant is small, and the DIBL decreases as the dielectric constant increases, and it can be observed that the DIBL appears constant when the high-*k* dielectric constant is 20 or higher. As seen in (2.15) and Figure 5,

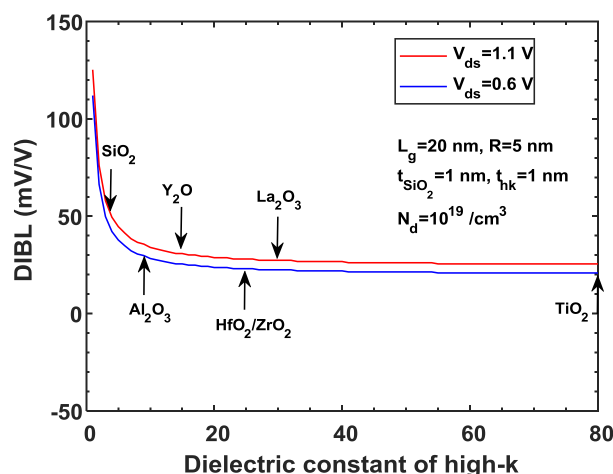

Figure 5. DIBLs for dielectric constant of high-*k* with the drain voltage as a parameter.

the DIBL changed according to the drain voltage, and the DIBL increased as the drain voltage increased. If the high-*k* dielectric constant is as small as 3.9 like SiO_2, the rate of change of DIBL for the change of the drain voltage ($\triangle DIBL/\triangle V_{ds}$) is about 14.6 mV/V^2 under the conditions given in Figure 5, but the changing rate of DIBL was maintained with 10 mV/V^2 when the high-*k* dielectric constant is 20 above.

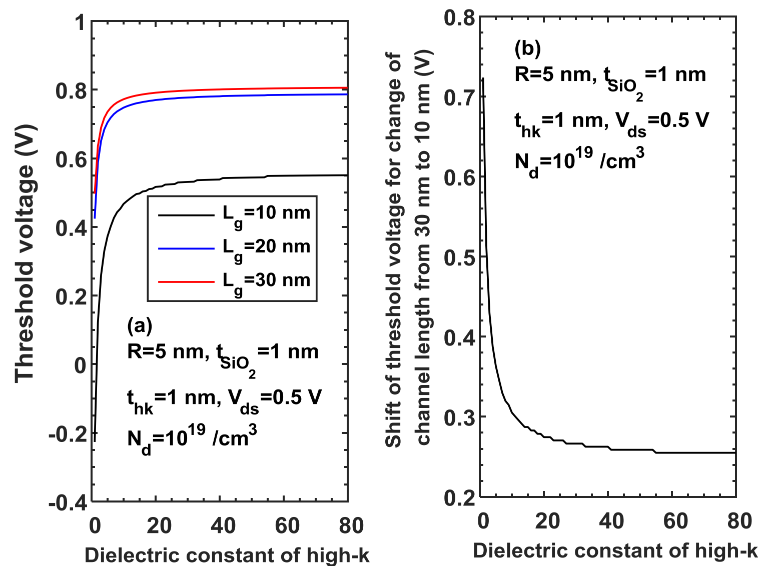

Figure 6. (a) Threshold voltages and (b) threshold voltage shift for dielectric constant of high-*k* with the channel length as a parameter.

The change of the threshold voltage with respect to the high-*k* dielectric constant as a parameter of the channel length is shown in Figure 6(a). As seen from Figure 2 and Figure 6(a), a threshold voltage shift occurs and the threshold voltage decreases when the channel length decreases. As the channel length decreased, the degree of reduction increased significantly according to the high-*k* dielectric constant. As described above, a constant threshold voltage was exhibited regardless of the channel length when the high-*k* dielectric constant is 20 or more. The shift of the threshold voltage is shown in Figure 6(b) when the channel length decreases from 30 nm to 10 nm. As seen from Figure 6(b), the shift of the threshold voltage decreases as the dielectric constant of high-*k* increases. In particular, the shift of the threshold voltage is almost constant when the dielectric constant of high-*k* is 20 or more.

The change of DIBL according to the high-*k* dielectric constant as a parameter of the channel length is shown in Figure 7(a). The DIBL shows a large change according to the high-*k* dielectric constant when the channel length is very small such as about 10 nm. However, it can be observed that the change of high-*k* dielectric constant does not have a significant effect on DIBL when the channel length is increased to 30 nm. The change of DIBL (ΔDIBL) is shown in Figure 7(b) when the channel length changes from 30 nm to 10 nm. As seen from Figure 7(b), the change in DIBL was greatly reduced as the high-*k* dielectric constant increased. Like the threshold voltage, ΔDIBL was almost constant when the high-*k* dielectric constant was 20 or higher.

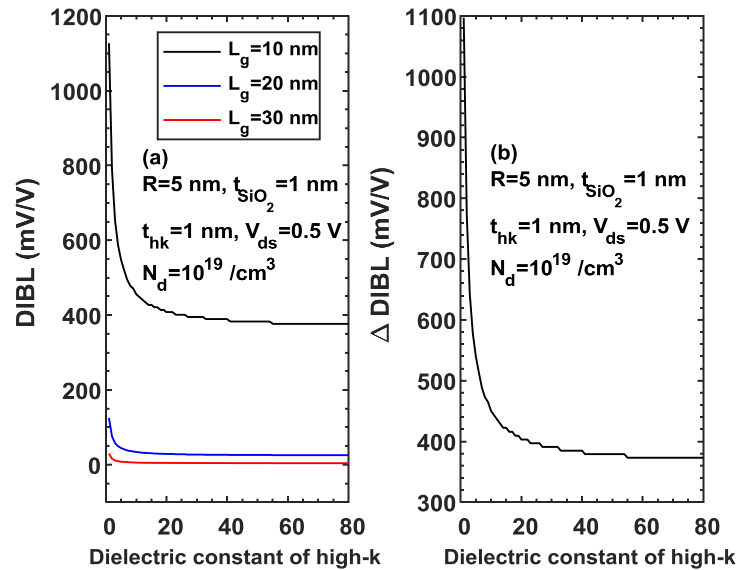

Figure 7. (a) DIBLs and (b) shift of DIBL for dielectric constant of high-*k* with the channel length as a parameter.

The reason for using high-*k* dielectric is to solve the difficulty in the process due to the reduction of the oxide film thickness. That is, the effective oxide thickness (EOT) can be increased by the ratio of the high-*k* dielectric constant and the SiO_2 dielectric constant of 3.9 [36]. Therefore, if the high-*k* oxide film is used, it will be possible to solve the difficulty in the process due to the reduction in the oxide film thickness. Here, we will observe the effect of the thickness of the high-*k* material on the threshold voltage. In Figure 8, the change of the threshold voltage with respect to the dielectric constant of high-*k* materials is shown with the thickness of the high-*k* material as a parameter. As shown in Figure 8(a), the threshold voltage increases as the dielectric constant of high-*k* material increases, but the rate of increase decreases rapidly, and the threshold voltage is maintained almost constant at a dielectric constant of above 20. In particular, if t_{hk} was decreased to 1 nm, even if the dielectric constant was 10 or more, the threshold voltage was maintained constantly regardless of the value of the high-*k* dielectric constant. Figure 8(a) shows that the threshold voltage changes sensitively to the change of dielectric constant as the thickness of high-*k* material increases, and the shift of threshold voltage decreases as the dielectric constant increases when the thickness of high-*k* material is changed from t_{hk} = 1 nm to t_{hk} = 5 nm as shown in Figure 8(b).

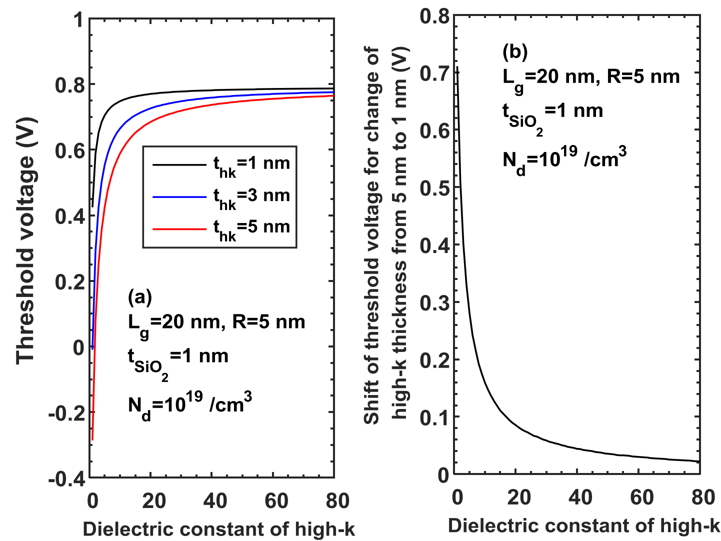

Figure 8. (a) Threshold voltages and (b) threshold voltage shift for dielectric constant of high-*k* with the thickness of high-*k* dielectric as a parameter.

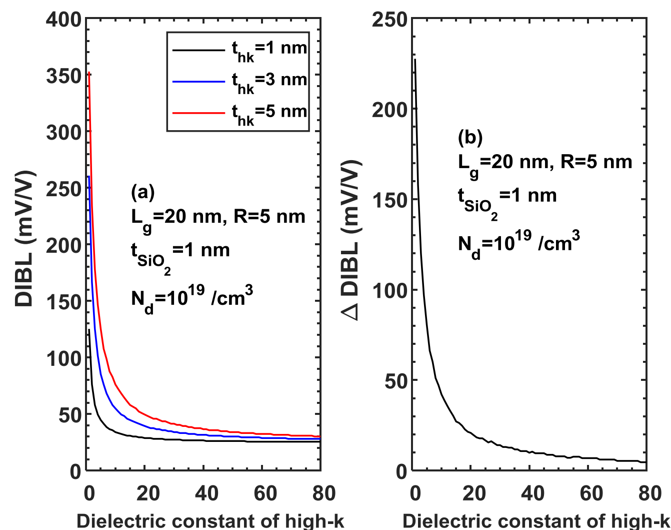

Figure 9. (a) DIBLs and (b) shift of DIBL for dielectric constant of high-*k* with the thickness of high-*k* dielectric as a parameter.

Figure 9 shows the change of the DIBL according to the dielectric constant with the thickness of the high-*k* material as a parameter. Figure 9(a) shows that the DIBL decreased as the dielectric constant of the high-*k* material increased and the thickness decreased. As explained in Figure 8, it could be observed that if t_{hk} is decreased to 1 nm, the change in DIBL according to the dielectric constant is negligibly small even if the high-*k* dielectric constant is 10 or more. Figure 9(b) shows the change of DIBL according to the dielectric constant when the thickness of high-*k* is changed from t_{hk} = 1 nm to t_{hk} = 5 nm. The effect of the thickness change of the high-*k* material on DIBL is very small as the dielectric constant increases.

Comparing Figure 6 and Figure 8, the change in the threshold voltage according to the dielectric

constant of the high-*k* material has a greater influence on the channel length than the change in the thickness of the high-*k* material. That is, the threshold voltage shift of about 0.26 V appeared when the channel length changed from 30 nm to 10 nm for the high-*k* dielectric of 20 or more, but the threshold voltage shift of about 0.05 V was only occurring when the thickness of the high-*k* dielectric changed from 1 nm to 5 nm. As seen from the comparison between Figure 7 and Figure 9, DIBL shift of about 380 mV/V appears when the channel length changes from 30 nm to 10 nm with a high-*k* dielectric constant of 20 or more. However, only the change of the DIBL of about 20 mV/V occurred when the dielectric thickness changes from 1 nm to 5 nm.

4. Conclusions

In this study, the analytical models of threshold voltage and DIBL were proposed to analyze the change in the threshold voltage and DIBL among the short channel effects of JLCSG MOSFETs using a stacked high-*k* dielectric as an oxide layer. They matched very well as a result of comparison with other papers. As scaling progresses, problems such as difficulty in process and short channel effects occur due to a reduction in the thickness of the oxide film according to the channel length. In this paper, the change of the threshold voltage and DIBL according to the dielectric constant of the high-*k* materials was observed using the proposed model with the channel length and thickness of the high-*k* dielectric as parameters. The shifts of threshold voltage and DIBL are 0.39 V and 577 mV/V, respectively, when the channel length decreases from 30 nm to 10 nm if SiO_2 is used as a high-*k* material, whereas it can be seen that those decrease to 0.27 V and 403 mV/V, respectively when the dielectric constant of the stacked high-*k* material is increased to 20. In addition, considering the changes in the thickness of the high-*k* dielectric, the shifts of threshold voltage and DIBL are 0.33 V and 97.0 mV/V, respectively when the thickness of the high-*k* dielectric decreases from 1 nm to 5 nm if SiO_2 is used as a high-*k* material. On the other hand, it was found that those decreased to 0.086 V and 20.8 mV/V, respectively when the dielectric constant of the high-*k* material increased to 20. As described above, the short-channel effect can be reduced in JLCSG MOSFETs by using a stacked high-*k* dielectric as the gate oxide. It was found that the proposed models excellently analyzed the threshold voltage and DIBL.

Conflict of interest

All authors declare no conflicts of interest in this paper.

References

1. Afzalian A (2021) Ab initio perspective of ultra-scaled CMOS from 2D-material fundamentals to dynamically doped transistors. *npj 2D Mater Appl* 5: 1–13. https://doi.org/10.1038/s41699-020-00181-1
2. Xu K, Chen D, Yang F, et al. (2017) Sub-10 nm Nanopattern Architecture for 2D Material Field-Effect Transistor. *Nano Lett* 17: 1065–1070. https://doi.org/10.1021/acs.nanolett.6b04576
3. Menduratta N, Tripathi SL (2020) A review on performance comparison of advanced MOSFET structures below 45 nm technology node. *J Semicond* 41: 061401. https://doi.org/10.1088/1674-4926/41/6/061401
4. Lee J, Choi K (2016) Trend and issues of the bulk FinFET. *Vacuum Magazine* 3: 16–21. https://doi.org/10.5757/vacmac.3.1.16

5. Chiarella T, Kubicek S, Rosseel E, et al. (2016) Towards High Performance Sub-10 nm finW Bulk FinFET Technology. *2016 46th European Solid-State Device Research Conference (ESSDERC)*, Lausanne Switzerland, 131–134. https://doi.org/10.1109/ESSDERC.2016.7599605
6. Zhao D, Tian Z, Liu H, et al. (2020) Realizing an Omega-Shaped Gate MoS2 Field-Effect Transistor Based on a SiO2/MoS2 Core-Shell Heterostructure. *ACS Appl Mater Inter* 12: 14308–14314. https://doi.org/10.1021/acsami.9b21727
7. Agarwal A, Pradhan PC, Swain BP (2020) Corrected Drain Current Model for Schottky Barrier Cylindrical Gate All Around FET Considering Quantum Mechanical Effects. *Telecommunications and Radio Engineering* 79: 433–442. https://doi.org/10.1615/TelecomRadEng.v79.i5.60
8. Dargar A, Srivastava VM (2021) Performance Comparison of Stacked Dual-Metal Gate Engineered Cylindrical Surrounding Double-Gate MOSFET. *Int J Electron Telec* 67: 29–34.
9. Sharma S, Chaudhury K (2012) A Novel Technique for Suppression of Corner Effect in Square Gate All Around MOSFET. *Electrical and Electronic Engineering* 2: 336–341.
10. Lee J, Kang M (2021) TID Circuit Simulation in Nanowire FETs and Nanosheet FETs. *Electronics* 10: 956. https://doi.org/10.3390/electronics10080956
11. Colinge JP, Kranti A, Yan R, et al. (2011) Junctionless Nanowire Transistor (JNT): Properties and design guidelines. *Solid-State Electronics* 65: 33–37. https://doi.org/10.1016/j.sse.2011.06.004
12. Nowbahari A, Roy A, Marchetti L (2020) Junctionless Transistors: State-of-the-Art. *Electronics* 9: 1174. https://doi.org/10.3390/electronics9071174
13. Lee C, Borne A, Ferain I, et al. (2010) High-Temperature Performance of Silicon Junctionless MOSFETs. *IEEE T Electron Dev* 57: 620–625. https://doi.org/10.1109/TED.2009.2039093
14. Huda ARN, Arshad MKM, Othman N, et al. (2015) Impact of Size Variation in Junctionless vs Junction Planar SOI n-MOSFET Transistor. *2015 IEEE Regional Symposium on Micro and Nanoelectronics(RSM)*, Kuala Terengganu, 1–4. https://doi.org/10.1109/RSM.2015.7354983
15. Jung H (2019) Analysis of Threshold Voltage Roll-off and Drain Induced Barrier Lowering in Junction-Based and Junctionless Double Gate MOSFET. *Journal of the Korean Institute of Electrical and Electronic Material Engineers* 32: 104–109. https://doi.org/10.21660/2019.55.4510
16. Jung H (2021) Analysis of subthreshold swing in junctionless double gate MOSFET using stacked high-k gate oxide. *International Journal of Electrical and Computer Engineering* 11: 240–248. https://doi.org/10.11591/ijece.v11i1.pp240-248
17. Manikanda S, Balamurugan NB, Nirmal D (2020) Analytical Model of Double Gate Stacked Oxide Junctionless Transistor Considering Source/Drain Depletion Effetcs for CMOS Low Power Application. *Silicon* 12: 2053–2063. https://doi.org/10.1007/s12633-019-00280-9
18. Haque M, Kabir H, Adnan MR (2021) Analytical modelling and verification of potential profile of DG JLFET with and without stack oxide. *Int J Electron* 108: 819–840. https://doi.org/10.1080/00207217.2020.1818842
19. Baral K, Singh PK, Kumar S, et al. (2020) Ultrathin body nanowire hetero-dielectric stacked asymmetric halo doped junctionless accumulation model MOSFET for enhanced electrical chracteristics and negative bias stability. *Superlattice Microst* 138: 106364. https://doi.org/10.1016/j.spmi.2019.106364
20. Swain SK, Biswal SM, Das SK, et al. (2020) Performance Comparison of InAs Based DG-MOSFET with Respect to SiO2 and Gate Stack Configuration. *Nanoscience & Nanotechnology-Asia* 10: 419–424. https://doi.org/10.2174/2210681209666190919094434

21. Panchanan S, Maity R, Maity NP (2021) Modeling, Simulation and Analysis of Surface Potential and Threshold Voltage: Application to High-K Material HfO_2 Based FinFET. *Silicon* 13: 3271–3289. https://doi.org/10.1007/s12633-020-00607-x
22. Maity NP, Maity R, Maity S, et al (2019) A New Surface Potential and Drain Current Model of Dual Material Gate Short Channel Metal Oxide Semiconductor Field Effect Transistor in Subthreshold Regime: Application to High-K material HfO_2. *J Nanoelectron Optoe* 14: 868–876. https://doi.org/10.1166/jno.2019.2547
23. Rasol MFM, Hamid FKA, Johari Z, et al. (2019) Stacking SiO2/High-k Dielectric Material in 30 nm Junction-less Nanowire Transistor Optimized Using Taguchi Method for Lower Leakage Current. *2019 IEEE Regional Symposium on Micro and Nanoelectronics (RSM)*, Pahang, 1–4. https://doi.org/10.1109/RSM46715.2019.8943545
24. Darwin S, Samuel TSA, Vimala P (2020) Impact of two gate oxide with no junction metal oxide semiconductor field effect transistor- an analytical model. *Physica E: Low-dimensional Systems and Nanostructures* 118: 113803. https://doi.org/10.1016/j.physe.2019.113803
25. Kosmani NF, Mamid FA, Razali MA (2020) Effect of High-k Dielectric Materials on Electrical Performance on Double Gate and Gate-All-Around MOSFET. *Int J Integ Eng* 12: 81–88.
26. Gupta S, Pandey N., Gupta RS (2020) Investigation of Dual-Material Double Gate Junctionless Accumulation-Mode Cylindrical Gate All Around(DMDG-JLAM-CGAA) MOSFET with High-k Gate Stack for Low Power Digital Applications. *2020 IEEE 17th india Council International Conference (INDICON)*, New Delhi 1–4. https://doi.org/10.1109/INDICON49873.2020.9342380
27. Gupta V, Awasthi H, Kumar N et al. (2021) A Novel Approach to Model Threshold Voltage and Subthreshold Current of Graded-Doped Junctionless-Gate-All-Around(GD-JL-GAA) MOSFETs. *Silicon* 1–9. https://doi.org/10.1007/s12633-021-01084-6
28. Hu G, Xiang P, Ding Z, et al. (2014) Analytical Models for Electric Potential, Threshold Voltage, and Subthreshold Swing of Junctionless Surrounding-Gate Transistors. *IEEE T Electron Dev* 61: 688–695. https://doi.org/10.1109/TED.2013.2297378
29. Maduagwu UA, Srivastava VM (2019) Analytical Performance of the Threshold Voltage and Subthreshold Swing of CSDG MOSFET. *Journal of Low Power Electronics and Applications* 9: 10. https://doi.org/10.3390/jlpea9010010
30. Li C, Zhuang Y, Di S., et al. (2013) Subthreshold Behavior Models for Nanoscale Short-Channel Junctionless Cylindrical Surrounding-Gate MOSFETs. *IEEE T Electron Dev* 60: 3655–3662. https://doi.org/10.1109/TED.2013.2281395
31. Duksh YS, Singh B, Gola D, et al. (2021) Subthreshold Modeling of Graded Channel Double Gate Junctionless FETs. *Silicon* 13: 1231–1238. https://doi.org/10.1007/s12633-020-00514-1
32. Gupta SK (2015) Threshold voltage model of junctionless cylindrical surrounding gate MOSFETs including fringing field effects. *Supperlattices and Microstructures* 88: 188–197. https://doi.org/10.1016/j.spmi.2015.09.001
33. Ehteshanuddin M, Loan SA, Rafat M (2017) Excellent DIBL Immunity in Junctionless Transistor on a High-k Buried Oxide. *2017 IEEE 14th india Council International Conference (INDICON)*, Roorke, 1–4. https://doi.org/10.1109/INDICON.2017.8487497
34. Bhagat K, Patil GC (2020) Engineering substrate doping in bulk planar junctionless transistor: Scalability and variability study. *Engineering Research Express* 2: 025028. https://doi.org/10.1088/2631-8695/ab91f7

35. Lagraf F, Rechem D, Guergouri K, et al. (2019) Channel Length Effect on Subthreshold Characteristics of Junctionless Trial Material Cylindrical Surrounding-Gate MOSFET with High-k Gate Dielectrics. *Journal of Nano- and Electronic Physics* 11: 02011. https://doi.org/10.21272/jnep.11(2).02011
36. Clark RD (2014) Emerging Applications for High K Materials in VLSI Technology. *Materials* 7: 2913–2944. https://doi.org/10.3390/ma7042913

Appendix

A. Analytical threshold voltage

If $H = -\phi_{ms} + \dfrac{qN_d R}{2C_{ox}} + \dfrac{qN_d R^2}{4\varepsilon_{si}} - V_F$,

$$\begin{aligned}
\phi_{\min} = \phi(0, z_{\min}) &= V_{gs} + H + C_1 \exp\left(\frac{\alpha_1 z_{\min}}{R}\right) + D_1 \exp\left(-\frac{\alpha_1 z_{\min}}{R}\right) \\
&= V_{gs} + H + C_1 \exp\left(\frac{\alpha_1}{R}\frac{R}{2\alpha_1}\ln\left(\frac{D_1}{C_1}\right)\right) + D_1 \exp\left(-\frac{\alpha_1}{R}\frac{R}{2\alpha_1}\ln\left(\frac{D_1}{C_1}\right)\right) \\
&= V_{gs} + H + 2\sqrt{C_1 D_1} \\
&= V_{gs} + H + \left(1/\sinh\left(-\lambda_1\right)\right)\sqrt{\left[A\left(\exp\left(-\lambda_1\right)-1\right)-B\right]\left[A\left(1-\exp\left(\lambda_1\right)\right)+B\right]} \\
&= V_{gs} + H + \left(1/\sinh\left(-\lambda_1\right)\right)\sqrt{\left[(XV_{gs}+Y)\left(\exp\left(-\lambda_1\right)-1\right)-B\right]\left[(XV_{gs}+Y)\left(1-\exp\left(\lambda_1\right)\right)+B\right]} \\
&= V_{gs} + H + \left(1/\sinh\left(-\lambda_1\right)\right)\sqrt{\begin{aligned}&X^2\left(\exp\left(-\lambda_1\right)-1\right)\left(1-\exp\left(\lambda_1\right)\right)V_{gs}^2 + \\ &\left(Y\left(1-\exp\left(\lambda_1\right)\right)+B\right)\left(\exp\left(-\lambda_1\right)-1\right)XV_{gs} + \\ &\left(Y\left(\exp\left(-\lambda_1\right)-1\right)-B\right)\left(1-\exp\left(\lambda_1\right)\right)XV_{gs} + \\ &\left(Y\left(\exp\left(-\lambda_1\right)-1\right)-B\right)\left(Y\left(1-\exp\left(\lambda_1\right)\right)+B\right)\end{aligned}} \\
&= V_{gs} + H + \left(1/\sinh\left(-\lambda_1\right)\right)\sqrt{a_1 V_{gs}^2 + a_2 V_{gs} + a_3} = 0
\end{aligned} \tag{A-1}$$

$$\begin{aligned}
X &= \frac{-2}{J_0^2(\alpha_1) + J_1^2(\alpha_1)}\frac{J_1(\alpha_1)}{\alpha_1} \\
Y &= \left(-\phi_{MS} + \frac{qN_D R}{2C_{ox}} + \frac{qN_D R^2}{4\varepsilon_{si}}\right) + \frac{qN_D}{2\varepsilon_{si}}\frac{1}{J_0^2(\alpha_1) + J_1^2(\alpha_1)}\frac{\alpha_1 J_1(\alpha_1) - 2J_2(\alpha_1)}{\left(\alpha_1 / R\right)^2} \\
B &= \frac{2V_{ds}}{J_0^2(\alpha_1) + J_1^2(\alpha_1)}\frac{J_1(\alpha_1)}{\alpha_1} = -XV_{ds} \\
a_1 &= X^2\left(\exp\left(-\lambda_1\right)-1\right)\left(1-\exp\left(\lambda_1\right)\right) \\
a_2 &= \left(Y\left(1-\exp\left(\lambda_1\right)\right)+B\right)\left(\exp\left(-\lambda_1\right)-1\right)X + \left(Y\left(\exp\left(-\lambda_1\right)-1\right)-B\right)\left(1-\exp\left(\lambda_1\right)\right)X \\
a_3 &= \left(Y\left(\exp\left(-\lambda_1\right)-1\right)-B\right)\left(Y\left(1-\exp\left(\lambda_1\right)\right)+B\right)
\end{aligned} \tag{A-2}$$

If you find V_{gs} using the quadratic formula of (A-1), this is V_{th} of (2.14).

B. Analytical DIBL

The DIBL is defined as follows.

$$DIBL = -\frac{dV_{th}}{dV_{ds}}$$

Therefore, it can be found by differentiating (14) by V_{ds}. In (14), the only variables for V_{ds} are a_2 and a_3 with B, so

$$DIBL = -\frac{dV_{th}}{dV_{ds}} = \frac{1}{2\left[\frac{a_1}{\sinh^2(\lambda_1)} - 1\right]}\left\{\left(\frac{1}{\sinh^2(\lambda_1)}\right)\frac{da_2}{dV_{ds}} - \frac{\left\{\begin{array}{l}\left(\frac{a_2}{\sinh^2(\lambda_1)} - 2H\right)\left(\frac{1}{\sinh^2(\lambda_1)}\right)\frac{da_2}{dV_{ds}} - \\ 2\left(\frac{a_1}{\sinh^2(\lambda_1)} - 1\right)\left(\frac{1}{\sinh^2(\lambda_1)}\right)\frac{da_3}{dV_{ds}}\end{array}\right\}}{\sqrt{\begin{array}{l}\left[a_2/\sinh^2(\lambda_1) - 2H\right]^2 - \\ 4\left[a_1/\sinh^2(\lambda_1) - 1\right]\left[a_3/\sinh^2(\lambda_1) - H^2\right]\end{array}}}\right\} \tag{B-1}$$

In (B-1), the derivative of a_2 and a_3 with respect to V_{ds} is obtained using (A-2) as followings.

$$\begin{aligned}\frac{da_2}{dV_{ds}} &= -X^2\left(\exp(-\lambda_1) + \exp(\lambda_1) - 2\right) \\ \frac{da_3}{dV_{ds}} &= -XY\left(\exp(-\lambda_1) + \exp(\lambda_1) - 2\right) - 2X^2V_{ds}\end{aligned} \tag{B-2}$$

If (B-2) is substituted for (B-1), the DIBL of (B-3) can be obtained.

$$DIBL = -\frac{1}{2\left[a_1 - \sinh^2(\lambda_1)\right]}\left\{\begin{array}{l}X^2\left(\exp(-\lambda_1) + \exp(\lambda_1) - 2\right) + \\ \frac{\left\{\begin{array}{l}\left(\frac{a_2}{\sinh^2(\lambda_1)} - 2H\right)\left(-X^2\left(\exp(-\lambda_1) + \exp(\lambda_1) - 2\right)\right) - \\ 2\left(\frac{a_1}{\sinh^2(\lambda_1)} - 1\right)\left(-XY\left(\exp(-\lambda_1) + \exp(\lambda_1) - 2\right) - 2X^2V_{ds}\right)\end{array}\right\}}{\sqrt{\left[a_2/\sinh^2(\lambda_1) - 2H\right]^2 - 4\left[a_1/\sinh^2(\lambda_1) - 1\right]\left[a_3/\sinh^2(\lambda_1) - H^2\right]}}\end{array}\right\} \tag{B-3}$$

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