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Research article

Electro-thermal modelling and Tj estimation of wire-bonded IGBT power module with multi-chip switches subject to wire-bond lift-off

Nicolas Degrenne*, Romain Delamea and Stefan Mollov

Power Electronic System division, Mitsubishi Electric R&D Centre Europe, 1 allée de Beaulieu, 35700 Rennes, France

*** Correspondence:** Email: n.degrenne@fr.merce.mee.com; Tel: +33223455815.

Abstract: Wire-bonded multi-chip IGBT power modules constitute the heart of high-current power electronic motor drives. The most common failure mechanism is the degradation of the top-side wires. This deterioration impacts the electrical path and the individual dies' temperature. The temperature is thus not only a stressor, but also a failure precursor. It is thus typically sensed in health monitoring methods based on damage-accumulation-models and failure precursors. One way to estimate the temperature is through the on-state voltage at low load current as a temperature sensitive electrical parameter. The on-state voltage being sensitive to the quality of the top-side connection, the obtained temperature estimate is drifting with degradation. This drift typically leads to under-estimating the temperature, thus reducing the precision of health monitoring. Drift compensation methods based on re-calibration are effective in single-chip switches, but their performances are not viable in multi-chip switches. This is due to the different temperature and current conditions during the calibration and the estimation phases. This paper addresses the relation between wire-bond degradation and temperature in multi-chip switches and proposes a simple model to explain and reproduce the electro-thermal behaviours. The model is based on experimental results where the degradation of wire-bonds is reproduced by cutting the wires sequentially. The model is further used to explain the drift in temperature estimation and the performance of the drift compensation methods based on re-calibration. Overall, the paper provides new results and understandings of the thermo-electrical behaviour of multi-chip power IGBT modules subject to wear-out.

Keywords: health monitoring; IGBT power module; power cycling; temperature estimation; wire-bond degradation

1. Introduction

Wire-bonded multi-chip IGBT power modules constitute the heart of high-current power electronic motor drives. They are used in many reliability-critical applications such as traction and wind energy. In these applications, they constitute a large proportion of the total number of failures [1]. The failure either causes the triggering of a detection and protection circuit or results in catastrophic failures such as explosion, eventually also damaging connected equipment. The general structure is presented in Figure 1. For most modules and mission profiles, the main wear-out failure mechanism is the degradation of the top-side wires as a consequence to thermo-mechanical stress [2]. It was found that cracks develop at the interface between the aluminium wires and the metallization of the dies. Ultimately, the wires lift off, and do not ensure electrical contact. This degradation process can be reproduced in power cycling test benches [3].

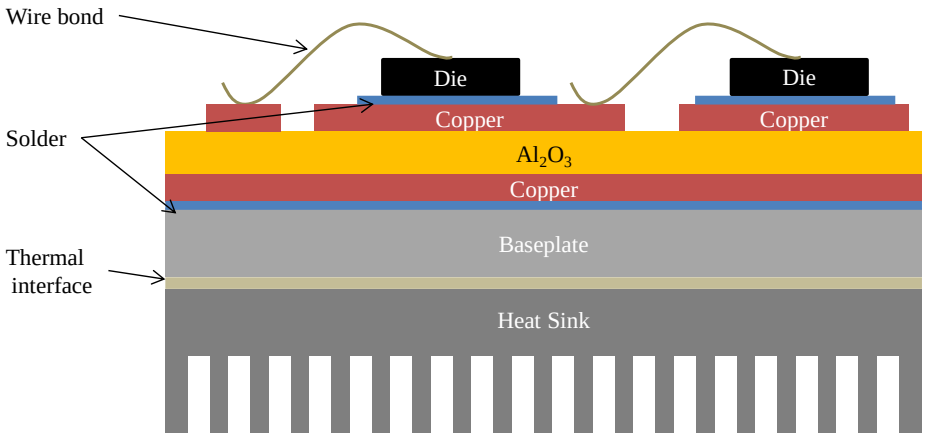

Figure 1. Typical structure of a power module used in a Power Electronic Converter (shown without encapsulation and casing).

Health monitoring is an enabler to condition-based maintenance which is of particular interest in availability-critical applications. This is especially true in industrial context where motors or other actuators are monitored. Health-monitoring can also accelerate the integration of new technologies such as SiC which present excellent performances but for which long term reliability is not yet acknowledged in all industries. A review on health monitoring applied to power modules [4] classifies health monitoring methods in two types:

- Damage-accumulation-based methods count and weight the temperature cycles.
- Condition-based methods follow the evolution of a failure precursor.

The review highlights the importance of temperature estimation in both approaches, as a value representative of stress, as a value representative of a failure, and as a value on which other measured parameters depend. In a multi-chip-switch power module, the individual die temperatures may vary as a consequence to thermal and/or electrical mismatch [5]. The degradation of the top-side connection modifies the individual electrical connections of the dies and thus also influence the temperature distribution within the different dies. This temperature distribution impacts the ageing

progression. It is thus of particular interest to know and understand the mechanisms of the temperature distribution when degradation increases. It is also critical to estimate the equivalent temperature in on-line applications, and to understand what it really represents, for example the average, minimum or maximum value of the different dies in parallel.

Estimating the temperature of the power dies was extensively studied in the past decades, with a strong focus on TSEPs (Temperature Sensitive Electrical Parameters) [6]. When multi-chip power modules are concerned, the individual die temperatures may vary as a consequence to thermal and/or electrical mismatch. In [7], a method is presented and evaluated for evaluating the temperature of each die independently with individual gate access. However, in the vast majority of large-current power modules, individual gate access is not available. One of the most common TSEPs is the on-state voltage Von. It can be implemented in different ways as listed in [8]. The method of Von at low-load current can be implemented in a wide majority of switching power cycling test benches that are used to investigate the failure mechanisms in a realistic way. The on-state voltage being sensitive to the quality of the top-side connection, the obtained temperature estimate is drifting with degradation. This drift naturally tends to under-estimate the temperature, thus reducing the capability of health monitoring with either of the two methods. Drift compensation methods based on re-calibration are possible in single-chip switches [8], but this paper will show that their performances are compromised in multi-chip switches.

This paper addresses the relation between wire-bond degradation and temperature in multi-chip modules and proposes a simple model to explain and reproduce the electro-thermal behaviours. The model is based on experimental results where the degradation of wire-bonds is reproduced by cutting the wires sequentially. The model is further used to explain the drift in temperature estimation and the performance of the drift compensation methods based on re-calibration. Overall, the paper provides new results and understandings of the thermo-electrical behaviour of multi-chip power IGBT modules subject to wear-out.

2. Materials and method

2.1. Experimental set-up

A six-pack 1200V/150A industrial power module was used as a DUT (Device Under Test). Each top-side IGBT die of this module is connected by 15 wires and 23 contacts as shown in Figure 2. The top-side dies were identified to be more often subject to wire-bond failures during power cycling. The three half-bridges of the module were connected in parallel so as to reproduce a multi-chip power module, each switch being constituted of 3 dies in parallel. The insulating gel was removed and the power module surface was black-painted. The DUT was mounted on a cold plate using a thermal interface foil covering only two third of the surface of the baseplate to create an initial temperature unbalance. The set-up was connected in a back-to-back power converter as previously described in [9] in unipolar modulation mode operating at 600 V.

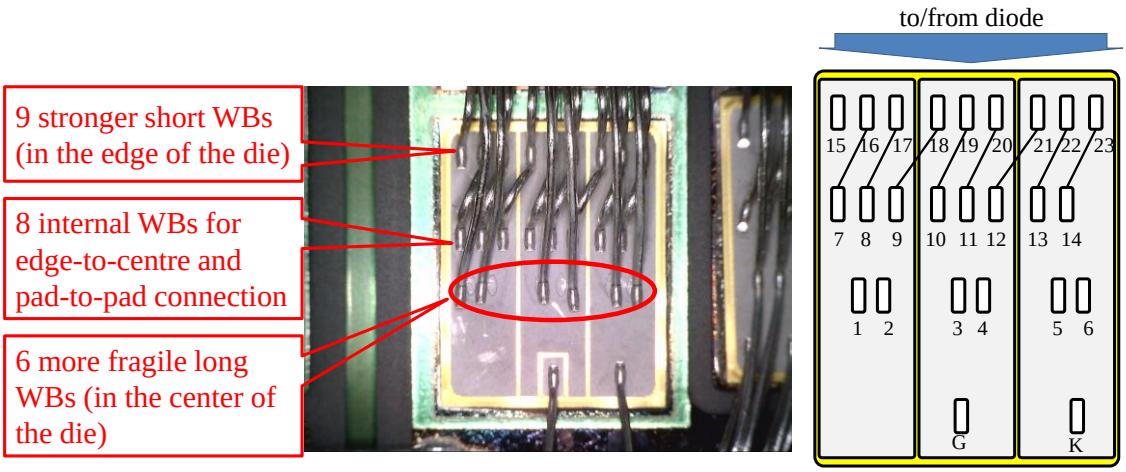

Figure 2. Photograph of a power cycled top-side die and corresponding routing.

A sequence of (re-)calibration, operation with measures of *Von* at low load current, and wire-bond cuts was performed as in Figure 3.

(Re)-calibration was performed by generating current pulses in a wide range (7 to 180 A) at various heat-sink temperatures. In between pulses, the current is null and the switches are not commutated, to prevent any self-heating. The obtained calibration data is used for estimation of *Tj* from *Von* and *Ion*. The data obtained with low current pulses in the range 7 to 13 A are used for temperature estimation. The data obtained with high-current pulses in the range 150 to 180 A are used for estimating the electrical resistance increase.

The power module was operated with a current of 100 A, a switching frequency of 13.3 kHz, and a duty-cycle of 0.5. The losses are thus a realistic combination of conduction and switching losses. A thermal IR (Infra-Red) camera was used to capture the average temperature of the area of each die. At regular intervals, the current was quickly reduced to preform measurements of *Von* at low load current. These measurements are used to estimate the temperature using the calibration data.

The initially hottest die 3 (due to the artificial thermal imbalance) was identified during the first temperature observation. If this thermally unbalanced power module would have been power cycled, it is most likely that the wires on the hottest die would have degraded faster, leading to their failure first. The wire-bonds of the initially hottest die were thus cut one by one, in a sequence previously studied in [3].

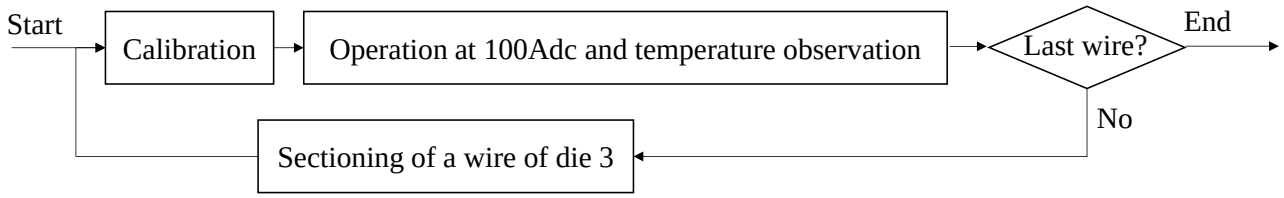

Figure 3. Experimental protocol.

3. Effect of wire-bond degradation on the temperature of individual dies

3.1. Results

The evolution of the die temperature, measured with the IR camera, is plotted in Figure 4 as a function of the number of wire-bond cuts on the initially hottest die 3. The error due to errors in area definition and to wire-bond masking is estimated to be ± 2 ℃. The temperature of die 3 is decreasing and the temperature of the two other dies are increasing as wires are sectioned. After 11 cuts, die 3 is not the hottest die anymore. Ultimately, when all the 15 wires of die 3 are cut, its temperature is only 67.5 ℃. The intuitive explanation for this temperature evolution is that, as the electrical connection of the die 3 is degraded, the current flow through it is reduced, and the conduction and switching losses are themselves reduced correspondingly. This hypothesis is supported by the evolution of the equivalent electrical resistance increase ΔReq in Figure 5. This curve was obtained based on the *Von* measurements at high current between each cut. The points follow a shape with 3 zones. During the first 6 cuts, i.e. corresponding to the long wires in Figure 2, the ΔReq increases from 0 to 0.3 mΩ. From 6 to 11 cuts corresponding to the first short wires, ΔReq is relatively constant. When the last wires are sectioned, the equivalent resistance increases in an accelerated way until 1 mΩ corresponding to the value when all the wires but the Kelvin connection (K in Figure 2) are cut.

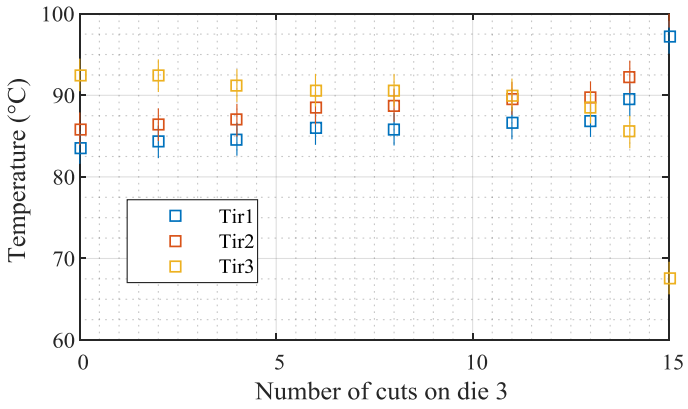

Figure 4. Temperature evolution of the 3 dies when the wires of die 3 are cut.

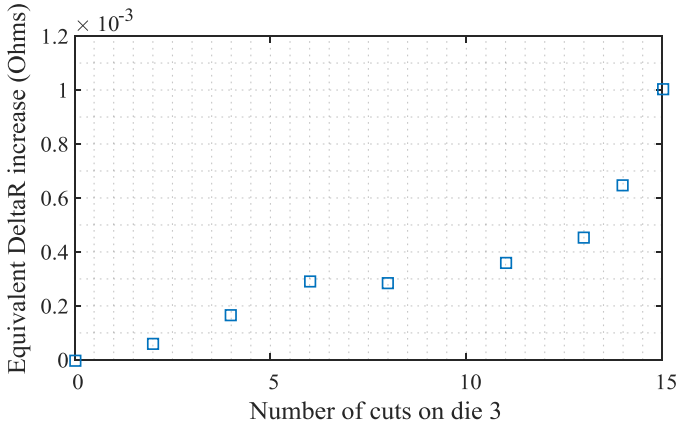

Figure 5. Equivalent resistance increase when the wires of die 3 are cut.

3.2. Modelling of the evolution of the temperature distribution

In this section, the intuitive sequence of electro-thermal effects resulting from wire-bond cut is modelled. First, the electrical interconnection is modelled electrically. Second, the dies are modelled electro-thermally. Both models are then combined.

3.2.1. Electrical model of the top-side interconnection

The main objective of this model is to estimate the electrical resistance increase Δ*R3* of the die 3. The input of the model is the equivalent electrical resistance increase Δ*Req* across the 3 parallel dies, measured with high-current pulses in the condition of negligible self-heating. This model assumes that the 3 dies have the same temperature (i.e. *Tji=Tc*) and the same linear static characteristics in the current of interest. The equivalent static characteristic of the 3 dies in parallel is thus expressed in the simple form (1), *A* and *B* being temperature-dependent parameters that are estimated based on the fitting of the *Von* measured during calibration at *Tc* and various high-current pulses in the range 110 A to 190 A.

$$V_{ON0} = \mathrm{A(Tc)}.I_{ON} + \mathrm{B(Tc)} \tag{1}$$

The corresponding equivalent and individual lumped models are shown in Figure 6. The equality between these models results in (2), where N is the number of dies in parallel.

$$\Delta R_3 = \Delta R_{EQ}.\frac{N^2}{1-(N-1)\frac{\Delta R_{EQ}}{A(Tc)}} \tag{2}$$

The evolution of ΔR3 as a function of cut wires is shown in Figure 7. After 15 cuts, the value of ΔR3 is 30 mΩ and not infinity, thanks to the remaining Kelvin connection. The evolution of the die temperatures, plotted as a function of the electrical resistance increase of die 3, Δ*R3*, is presented in Figure 8. The mean temperature is also displayed and is relatively constant, i.e. comprised between 87.5 and 90 ℃ during the whole experiment.

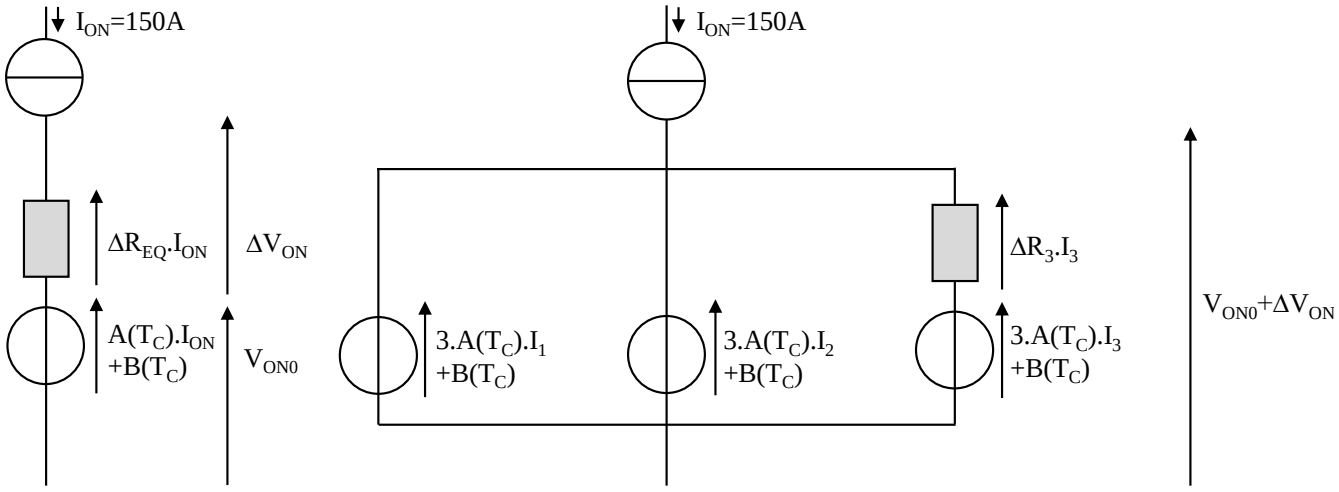

Figure 6. Equivalent (left) and individual (right) lumped models of the multi-chip power module with the electrical connection.

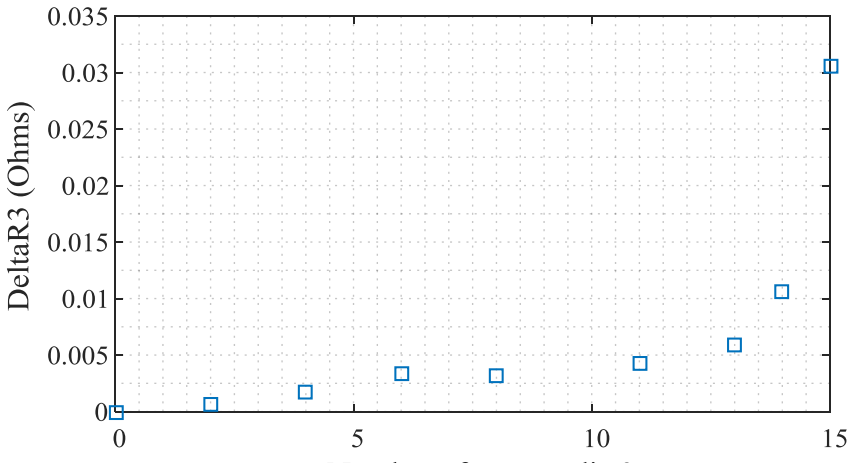

Figure 7. Evolution of the electrical resistance increase $\Delta R3$ of die 3 computed based on the equivalent resistance increase ΔReq.

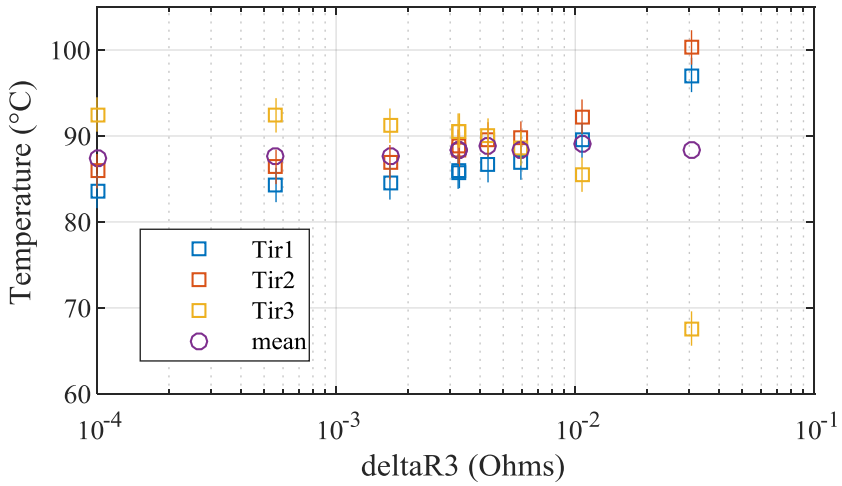

Figure 8. Temperature evolution of the 3 dies as a funtion of the computed electrical resistance increase $\Delta R3$ of die 3.

3.2.2. Electro-thermal model of the dies

Now that the electrical resistance increase $\Delta R3$ was computed, the objective of the electro-thermal model of the dies is to estimate the consequent voltage, currents, losses, and thermal distribution in the power module. The framework is illustrated in Figure 9 and forms a loop that is run until convergence. This section details the models and their outputs obtained after convergence.

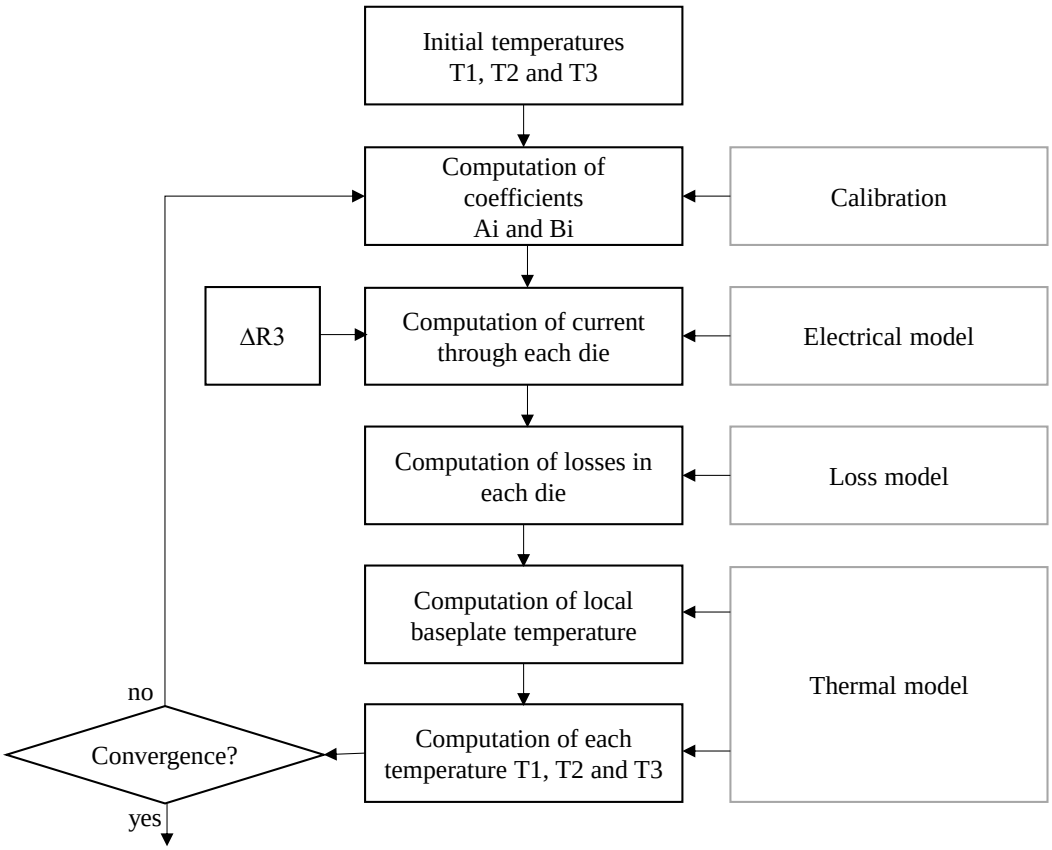

Figure 9. Framework for modeling the impact of the electrical resistance increase $\Delta R3$ on the temperature distribution.

3.2.3. Calibration and electrical models

The linear static curves according to the Eq. (1) are assumed with their individual dependency on the junction temperature Tji. The parameters A(Tji) and B(Tji) are extracted from the initial calibration in the region of operation, i.e. between 70 A and 130 A. Note that for a high number of cuts, the current distribution is expected to be very unbalanced, and the error in the parameters A and B is expected to increase.

For a given temperature distribution (Tj1, Tj2, Tj3) resulting in the coefficients (A1, A2, A3) and (B1, B2, B3), and a given electrical resistance increase (0, 0, ΔR3), the equivalent Von and individual Ii are derived using Kirchhoff's laws from the lumped electrical model in Figure 6, expressed by (3) and (4), and plotted in Figures 10 and 11 for the 3 IGBT dies. A similar calculation is performed for the bottom diodes, which losses also impact the case temperature.

$$Von = \frac{Itot.A_1.A_2.(A_3 + \Delta R_3) + B_2.A_1.(A_3 + \Delta R_3) + A_1.B_3.A_2 + B_1.A_2.(A_3 + \Delta R_3)}{A_2.(A_3 + \Delta R_3) + A_1.(A_3 + \Delta R_3) + A_1.A_2} \quad (3)$$

$$Ii = \frac{Von - B_i}{(A_i + \Delta R_i)} \quad (4)$$

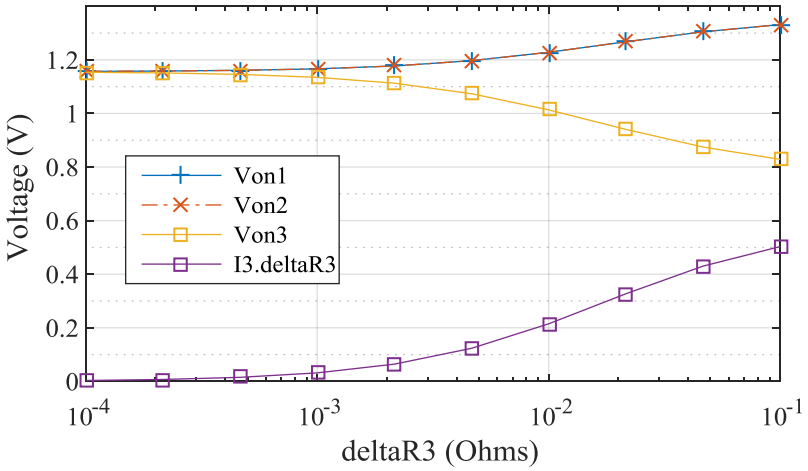

Figure 10. Modeled voltage evolutions for IGBT dies 1, 2 and 3, and for the voltage drop increase across the electrical connection of die 3.

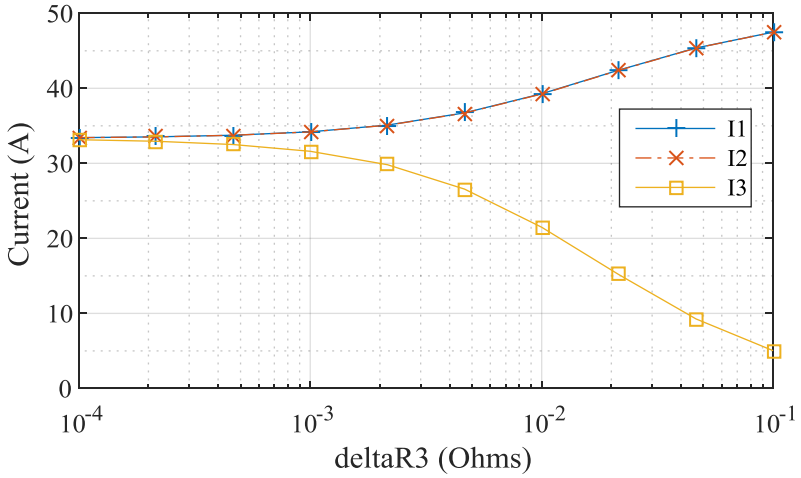

Figure 11. Modeled current evolutions for IGBT dies 1, 2 and 3.

3.2.4. Loss and thermal model

The losses in the IGBT and diode dies are expressed in (5) and (6), where α (= 0.5) is the duty-cycle, *Eon* (= 16.6e-3J) is the turn-on energy, *Eoff* (= 17.6e-3J) is the turn-off energy, *Err* (= 10.8e-3J) is the reverse recovery energy as indicated in the datasheet for 150 A. The losses in the IGBT dies are shown in Figure 12.

$$PlossI_i = \alpha.VonI.IonI_i + fsw.(Eon + Eoff).I_i/150 \quad (5)$$

$$PlossD_i = (1-\alpha).VonD.IonD_i + fsw.Err.I_i/150 \quad (6)$$

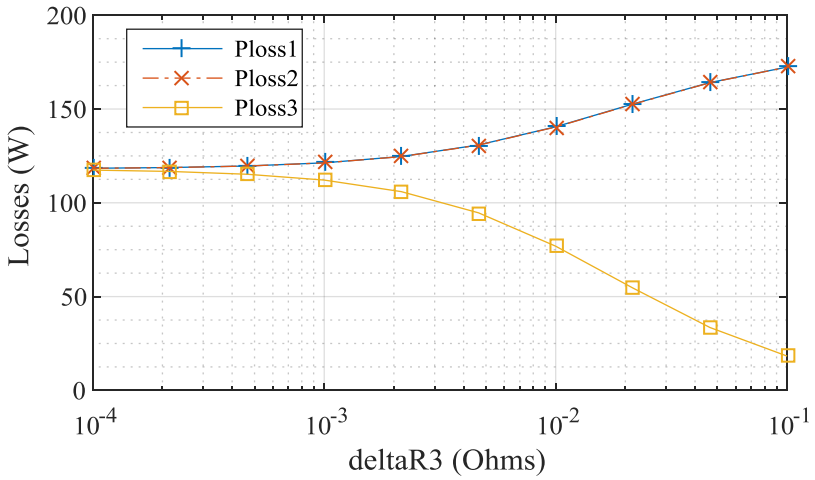

Figure 12. Losses in the IGBT dies.

The thermal model is presented in Figure 13. It distinguishes the 3 DBCs corresponding to the 3 legs, for which a specific case temperature is computed based on the losses of the IGBT and diode dies. The junction to case thermal resistances are defined based on the datasheet (i.e. 0.16 K/W for IGBT dies). The case to heat-sink thermistances are identified to obtain similar initial temperatures as in the experimental conditions. The resulting evolution of the temperature distribution is presented in Figure 14.

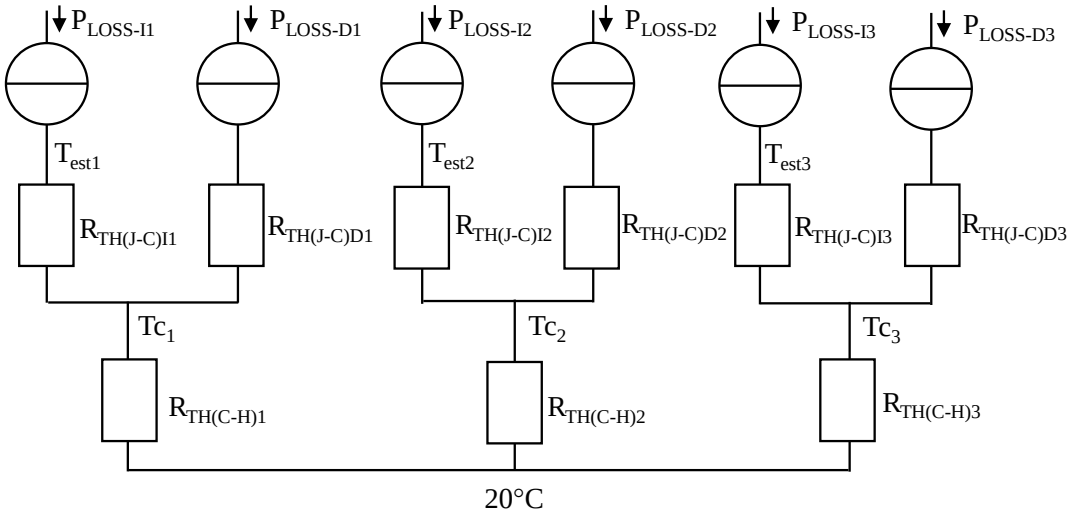

Figure 13. Lumped thermal model of the IGBT module.

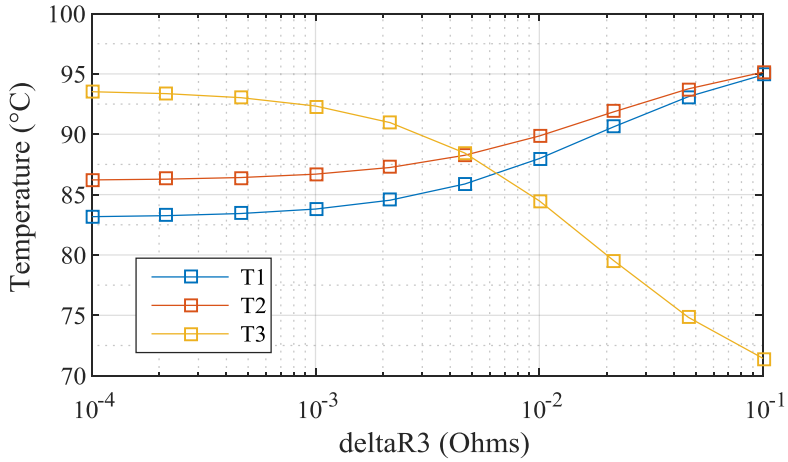

Figure 14. Estimated temperature based on the electro-thermal model.

3.3. Analysis

The superimposed measured and estimated temperatures are in Figure 15. The model estimates fit correctly the trend of the temperature evolution. For high number of wire-bond cuts, the measured temperature unbalance is more pronounced than the one estimated. The reason for this may be inaccuracies in the models, for example in the thermal model where a homogeneous heat-sink temperature of 20 ℃ was assumed. Overall, the qualitative trends are correct and confirm the mechanisms involved in the evolution of the temperature distribution.

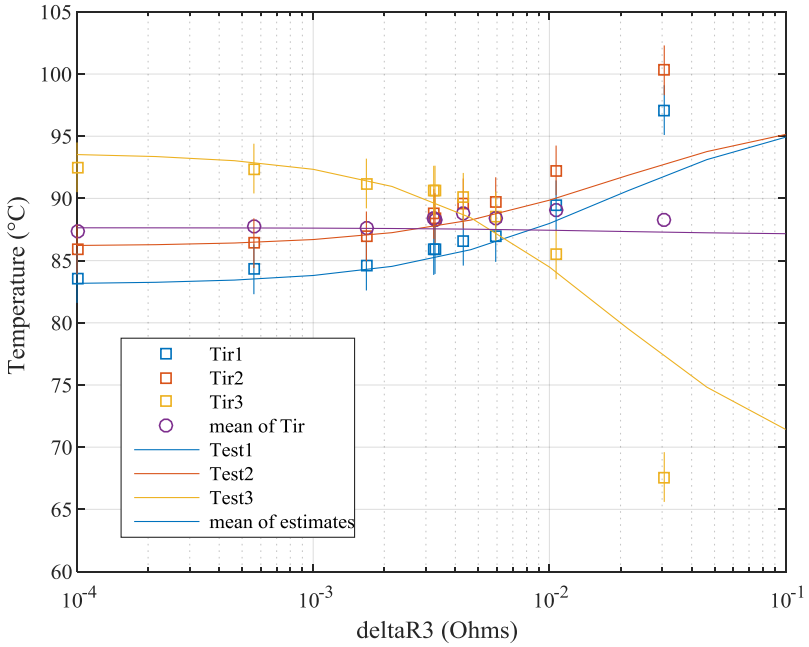

Figure 15. Comparison of measured and estimated temperatures.

4. Effect of wire-bond degradation on the temperature estimation with Von at low load current

4.1. Results

During power cycling in high-frequency test benches, temperature can be estimated in different ways. In [8], the temperature is estimated using Von at low load current pulses of 10 A. In the experiment described in this paper, a similar temperature estimation is studied. The initial calibration is used to establish the relation between *Von*, *Ion*, and *Tj*. The temperature was estimated with this method after each wire cut. The evolution of the equivalent junction *Tjeq* estimates is presented in Figure 16. Initially, in the absence of degradation, the *Tjeq* estimation is accurately identifying the mean temperature. However, as the degradation develops, the *Tjeq* is under-estimated. This phenomenon was already observed and explained in [8] in the case of a single-die switch. A method was proposed to correct the calibration model based on the estimation of the (equivalent) electrical resistance increase. The same compensation method was tested on the multi-chip module, and the results are also presented in Figure 16. As can be seen, the error is decreased by a factor of 2, but not fully cancelled as it was demonstrated in the case of a single chip module. The previously developed models are adapted and used in the next section to explain this observation.

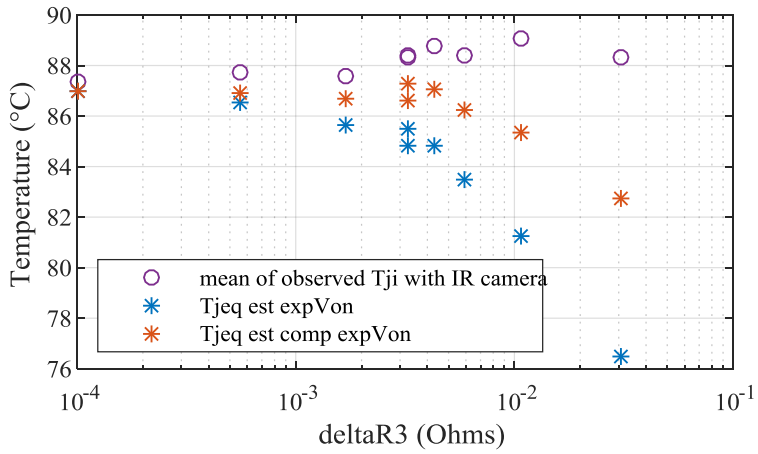

Figure 16. Comparison of average measured and estimated equivalent temperatures witout and with compensation of degradation.

4.2. Modelling of the temperature estimation

The process of temperature estimation was reproduced using the electrical models previously developed. The parameters *A(Tji)* and *B(Tji)* were identified based on the calibration data at low current using (1). For every value of $\Delta R3$ and corresponding previously estimated temperature, the equivalent *Von* was derived using (3) for a total current of 10 A. The equivalent *Von* was used together with the parameters *A* and *B* at low current to estimate the equivalent temperature. The resulting estimation is shown in Figure 17.

The process of compensation was also mimicked using the models. The Eq. (2) was inversed to find the equivalent electrical resistance increase at high current and constant die temperature. This value was used to correct the calibration coefficient *A* at low current, and the equivalent temperature with compensation was estimated as also shown in Figure 17. The modelled compensated temperature shows a reduction of the error of a factor 2, in agreement with the experimental results.

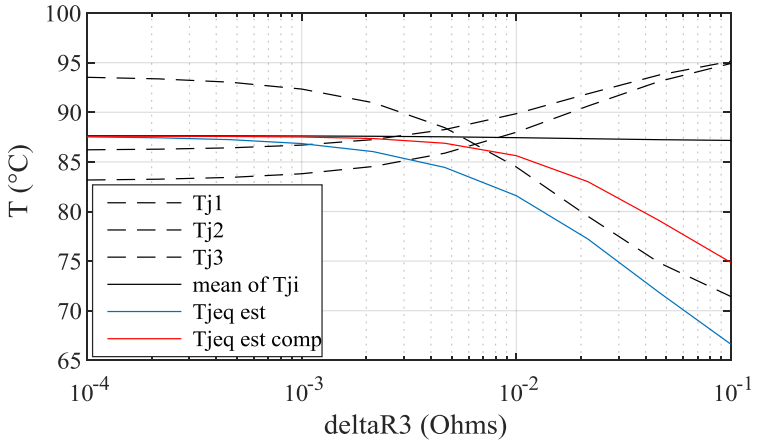

Figure 17. Comparison of estimated individual temperatures Tji and estimated equivalent temperatures Tjeq.

In order to explain this partial compensation, the equivalent resistance increase at low current and real measured temperatures is computed. For each value of $\Delta R3$ and of estimated individual temperatures, *Von* is calculated using (3). The *Von* increase is used to obtain the ΔReq increase at low current and to estimate the temperature.

The estimations of ΔReq at low current and at high current are in Figure 18. It can be seen that the ΔReq at low current is around double that of ΔReq at high current, mostly due to the differences in linearized static characteristics. For instance, in the low-current region, the *dI/dV* is lower (*A* is larger) and the result is a lower current unbalance, leading to more current in the degraded die, and a higher ΔReq. This is particularly enhanced by the experimental protocol consisting of cutting the wire-bonds of the same die 3, which leads to a high current unbalance.

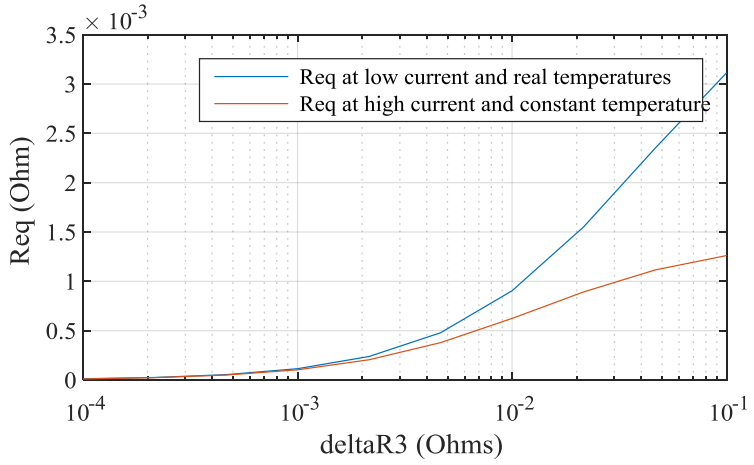

Figure 18. Comparison of the equivalent resistance increase estimated at low current and unbalanced temperatures (i.e. during the temperature estimation during operation), and estimated at high current and balanced temperatures (i.e. during assessment of degradation).

4.3. Analysis

Overall, the temperature estimates obtained directly through experimental measurement of *Von* and obtained with the models are plotted in Figure 19. The experimental and model results match relatively well. The description of mechanisms involved during the temperature estimation without and with compensation are thus well covered by the models. It is important to note that the scenario of sectioning the wire-bonds of a single die is a particular case, that leads to high current unbalances, and as a result, of low performance of the compensation due to very different estimations of ΔReq. In a more realistic scenario, less temperature unbalance and a higher performance of the compensation are expected.

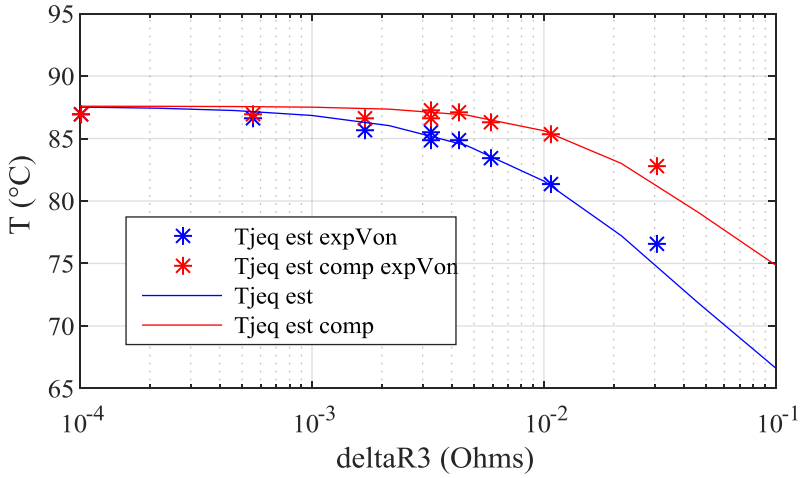

Figure 19. Comparison of the equivalent resistance increase estimated at low current and unbalanced temperatures (i.e. during the temperature estimation during operation), and estimated at high current and balanced temperatures (i.e. during assessment of degradation).

5. Conclusion

This paper addresses the temperature distribution and estimation in a multi-chip wire-bonded power module subject to degradation. A controlled and reproducible experimental protocol is used. First, it is shown that the degradation of the top-side connection of a specific die leads to the redistribution of the current towards healthy dies, and consequently tends to decrease its temperature. This negative feedback is modelled in this paper. It tends to equilibrate the lifetime of the different dies even in the presence of an initial imbalance. Second, Von at low load current as a TSEP under-estimates the equivalent temperature when the degradation propagates. A method of re-calibration based on the estimation at high current of the equivalent electrical resistance increase reduces the error of a factor of 2. This imperfect compensation is due to the different conditions during the phases of degradation estimation and temperature estimation. The obtained results should be considered as a worst-case, since the experimental protocol favours a high degradation unbalance.

In the future, it is first necessary to improve the temperature estimation method based on Von. Research directions includes correcting the measured electrical resistance increase with models, or

defining more efficient ways to perform calibration, for example that include compensation. It is also necessary to develop technologies to assess and eventually control the temperature of each die individually, which is proposed in [8] and will offer benefits in condition monitoring and reliability. Finally, the understanding of fault propagation in complex multi-chip systems will be useful to interpret power cycling results. It will contribute to design for reliability, health monitoring, diagnostics and prognostics of power electronic systems.

Conflict of interest

The authors declare that there is no conflict of interest.

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