AIMS Materials Science, 10(6): 965–980.
DOI: 10.3934/matersci.2023052
Received: 03 September 2023
Revised: 08 October 2023
Accepted: 12 October 2023
Published: 27 October 2023

http://www.aimspress.com/journal/Materials

Letter

Analysis and design of current mode logic based on CNTFET

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Abstract: In this letter we present a current mode gate based on differential pair as an application of carbon nanotube field effect transistors (CNTFETs). The proposed circuit has two output logic gates: one is NAND, and the other is AND. To simplify the circuit realization we use all CNTFETs of the same type, all with the same lengths and carbon nanotube symmetry indices (n,m). Complex circuits could be obtained in current mode replicating the differential pair CNTFET along the current path. The proposed procedure allows simulation of transfer characteristics from voltage input to current output but also from voltage input to voltage output. Moreover, we can measure simulated power dissipation and delay times.

Keywords: nanoelectronics; CNTFET; modeling; current mode logic; digital gates; advanced design system (ADS)

1. Introduction

We have been dealing with carbon nanotubes (CNTs) [1] and carbon nanotube field effect transistors (CNTFETs) [2–11] for many years now. In particular, we have studied extensively metal oxide semiconductor field effect transistor (MOSFET)-like CNTFETs for high-performance and low-power memory designs [12–22].

As is known, current mode logic has been developed since the beginning of digital electronics [23,24]. In this paper, we want to analyze the use of CNTFETs as current mode logic, because the present literature does not yet consider this type of application of CNTFETs.

In current mode circuits, the currents are used to represent signals. Current flow is maintained constant by switching currents between two paths. Current is passed from a logical gate to the following by enchaining logical gates on the same current flow. This enchaining is limited only by the sum of voltage drops on each gate compared to supply voltage.

We present a current mode AND-NAND logical gate, that is, a logical gate that presents both AND and NAND output.

The presentation is organized as follows. First, we present a brief review of the CNTFET model [2,3] used in the design. Then, we examine the proposed circuit, considering both static and transient analysis, and discuss the obtained results, together with the conclusions and future developments.

2. Materials and methods

2.1. A brief review of CNTFET model used

An exhaustive description of our CNTFET model is in our publications [2,3], and therefore the reader is requested to consult them.

The model, based on the hypothesis of ballistic transport, makes reference to [25] and the following improvements introduced in [26] to solve some numerical problems of the original paper [25].

In this section we just describe the main equations on which our current-voltage (I-V) model is based.

The total drain current I_{DS} in our model, defined by Eq 1, is expressed as in [27]:

$$I_{\mathrm{DS}} = \frac{4\mathrm{qkT}}{h}\sum_p \left[\ln\left(1+\exp\xi_{\mathrm{Sp}}\right) - \ln\left(1+\exp\xi_{\mathrm{Dp}}\right)\right] \tag{1}$$

where k is the Boltzmann constant, T is the absolute temperature, h is the Planck constant, and p is the number of sub-bands. $\xi_{\mathrm{Sp}}$and ξ_{Dp} have the expressions, shown in Eq 2:

$$\xi_{\mathrm{Sp}} = \frac{\mathrm{qV_{CNT}} - \mathrm{E_{Cp}}}{\mathrm{kT}} \text{ and } \xi_{\mathrm{Dp}} = \frac{\mathrm{qV_{CNT}} - \mathrm{E_{Cp}} - \mathrm{qV_{DS}}}{\mathrm{kT}} \tag{2}$$

where E_{Cp} represents the sub-bands conduction minima, V_{DS} is the drain-source voltage, and V_{CNT} is the surface potential.

In [7] we proposed, in order to evaluate V_{CNT}, the following approximation reported in Eq 3:

$$V_{\mathrm{CNT}} = \begin{cases} V_{\mathrm{GS}} & \text{for } \mathrm{V_{GS}} < \frac{E_C}{q} \\ V_{\mathrm{GS}} - \alpha\left(V_{\mathrm{GS}} - \frac{E_C}{q}\right) & \text{for } \mathrm{V_{GS}} \geq \frac{E_C}{q} \end{cases} \tag{3}$$

where E_C is the conduction band minimum for the first sub-band, and α is a parameter depending on V_{DS} voltage, CNTFET diameter and gate oxide capacitance C_{ox} [7,8].

In [3], where the output and transfer curves of the CNTFET simulated with our model are shown, we demonstrated that our model can well describe the behaviour of CNTFETs with a maximum value of V_{DS} equal to 3 V. For $V_{DS} \geq 3$ V, we assume that I_{DS} current has reached its saturation value, like the MOSFET model.

Moreover we also verified in [3] that only three sub-bands are sufficient to describe the output characteristics of CNTFET with a relative error less than 5%. This good agreement supports the validity of our approach.

Regarding the capacitance-voltage (C-V) model, an exhaustive description of our C-V model is widely described in [7,8], and therefore the reader is requested to consult these sources, in which the following expressions of quantum capacitances C_{GD} and C_{GS}, defined by Eq 4, are explained:

$$\begin{cases} C_{GD}=q\sum_p \frac{\partial n_{Dp}}{\partial V_{GS}}=q\sum_p \frac{\partial n_{Dp}}{\partial \xi_{Dp}}\frac{\partial \xi_{Dp}}{\partial V_{CNT}}\frac{\partial V_{CNT}}{\partial V_{GS}} \\ C_{GS}=q\sum_p \frac{\partial n_{Sp}}{\partial V_{GS}}=q\sum_p \frac{\partial n_{Sp}}{\partial \xi_{Sp}}\frac{\partial \xi_{Sp}}{\partial V_{CNT}}\frac{\partial V_{CNT}}{\partial V_{GS}} \end{cases} \quad (4)$$

In order to simulate correctly the CNTFET behaviour, we needed to estimate parasitic capacitances and inductances as well as the drain and source contact resistances.

We have achieved this goal using an empirical method exhaustively described in [2,3], where we explained that V_{FB}, R_D, R_S have been determined by a best-fit procedure between the measured and simulated values of I-V characteristics of the device, while the quantum capacitances have been computed from the charge in the channel. In this way, all elements of the CNTFET equivalent circuit, shown in Figure 1, are determined.

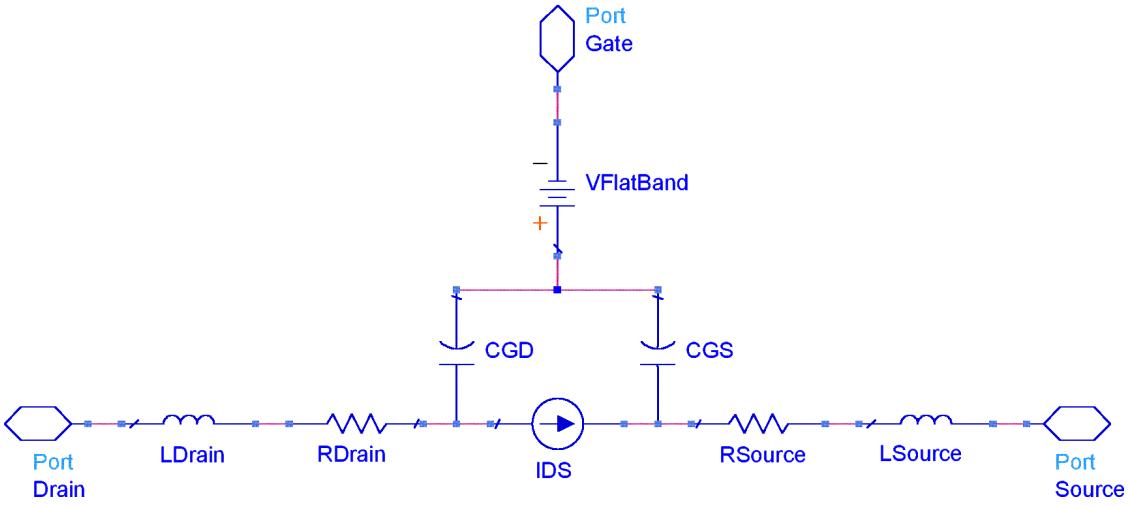

Figure 1. Equivalent circuit of an n-type CNTFET.

It is similar to a common MOSFET model and is characterized by the generator V_{FB}, indicated as VFlatBand, accounting for the flat band voltage, whose value is –0.0137 V; the quantum capacitance gate-source C_{GS}, indicated as CGS, and the quantum capacitance gate-drain C_{GD}, indicated as CGD. Moreover, having assumed a CNT length of 23 nm, the inductances of the CNT, LDrain and LSource, are both equal to 46 pH, and the resistors RDrain and RSource, in which the parasitic effects due to the electrodes are also included, are equal to 6362 and 21076 Ω, respectively.

Other authors [28,29] have then assumed these parameters fixed to constant and typical values (i.e., VFlatBand = 0 V [28] and RDrain = RSource = 25 kΩ [29]), thus losing the dependence on the CNT diameter.

Regarding the CNT quantum inductances, as shown in Figure 1 we have assumed them constant and split up into two inductances, LDrain and LSource, while the classical self-inductance, as it is known [28], can be ignored.

2.2. Proposed Circuit

The proposed circuit is shown in Figure 2 and has been developed using only one type of CNTFET, that is, all CNTs have the same diameter and length. This makes the circuit easier to realize than some CNTFET circuits proposed for other applications, where all CNTs have their own diameters and lengths. As values for CNTs, we choose indices (29,0) and length 23 nm.

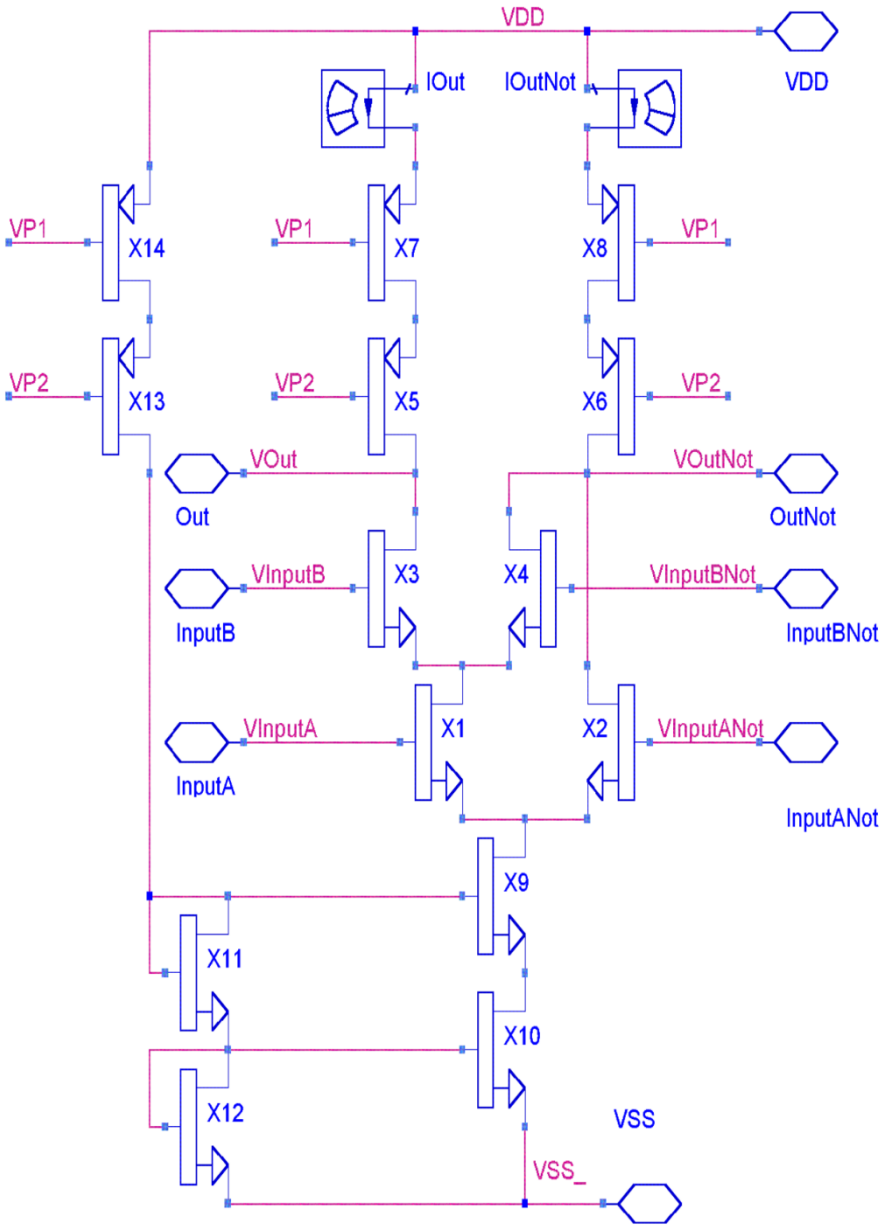

Figure 2. The proposed AND/NAND circuit.

As we have demonstrated in [21], the CNTs, when they are defect free, are identified by their length and their structural indices (n,m). Therefore these parameters are the key to identify the CNTFET behaviour. These parameters are not the only ones, since also contacts and parasitic effects

have their influence. We use VDD = 7 V and VSS = 0 V. The circuit has two input ports, named InputA and InputB. Signals at these ports drive, respectively, the CNTFETs of the pair X1 and X3.

The circuit also requires the negation of input signal applied at InputANot and InputBNot ports, driving, respectively, the CNTFETs of pair X2 and X4. The logic is based on current switching between X1 and X2 and between X3 and X4.

The current is regulated by the current mirror constituted by port X9, X10, X11, X12, while X5, X6, X7, X8 are load to the pairs X1, X2, X3, X4, while X13, X14 are load to the current mirror. The constant voltage generators, which drive points VP1 and VP2 and which could be shared by all current mode circuits on a chip, have been omitted.

At input ports, higher voltages are assumed as logical high.

The output is available as voltage at Out port and its negation at OutNot port. The output signal is available as current on the drain of CNTFET X5 and as voltage of the Out port. For the output, the higher voltages represent the logical high, but we will consider the higher current as logical low. In this way, the Out port, both for voltage and current levels, is the NAND of InputA and InputB port logical signals. Then, the voltage of OutNot port is the AND output signal as voltage, while the signal as current is the current at drain X6.

Please note that in the case of current output, this is the inverse of the usual definition, just because we inverted the definition of logical levels for output current. We prefer our definition in this presentation since we can label the Out port as NAND both for voltage and current, but we stress that this circuit is best used in current mode.

The circuit is not symmetric, so we will study the transfer curves separately for input InputA and InputB ports, and separately for output Out and OutNot ports. In the following, we name the port voltages using the prefix V: VInputA, VInputB, VOut, VOutNot. Meanwhile, with IOut we refer to the current flowing from X5 to X3, and with IOutNot we refer to the current flowing from X6 to X4 and X2.

To add more logical gates to in this circuit using the current mode logic, the new gates have to control the two currents coming, X5 and X6. This could be simply obtained by adding more CNTFET couples connected just beneath X5 and X6. In this case, of course, the polarization voltages VP1, VP2 and the voltage supply V_{DD} must be revised. Furthermore, the voltage thresholds of the input logical levels of the added gates will be higher than those of the our gate; and, to compensate for this shift, it would be necessary to add level shifter at the new inputs. While putting the focus at the currents, the current mode logic makes the addition of new gates more intricate than in the voltage mode logics.

Since we are interested in current mode, we will call IOut and IoutNot as current of Out and OutNot ports, improperly, since this is not current that crosses the ports, but usefully if we consider the circuit coupling in current mode logic.

3. Results and discussion

3.1. Static analysis

As said, since the circuit is not symmetric, we present in Figures 3–6 four transfer characteristics for output current and in Figures 7–10 for output voltages.

All simulations were carried out using the software Advanced Design System (ADS), which is compatible with the Verilog-A programming language [30].

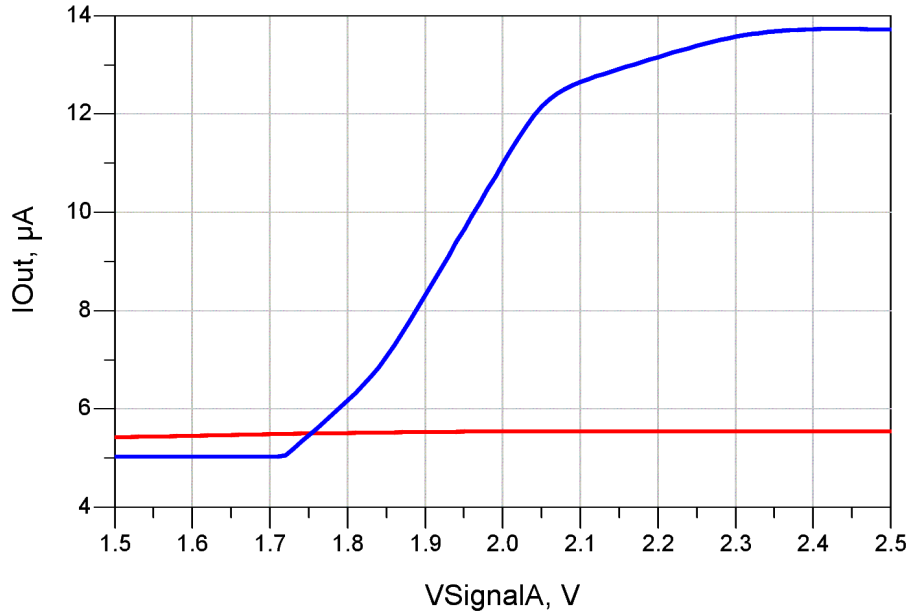

Figure 3. Current through the drain of the Out port versus voltage of InputA port when voltage of InputB port is low (red line) and high (blue line).

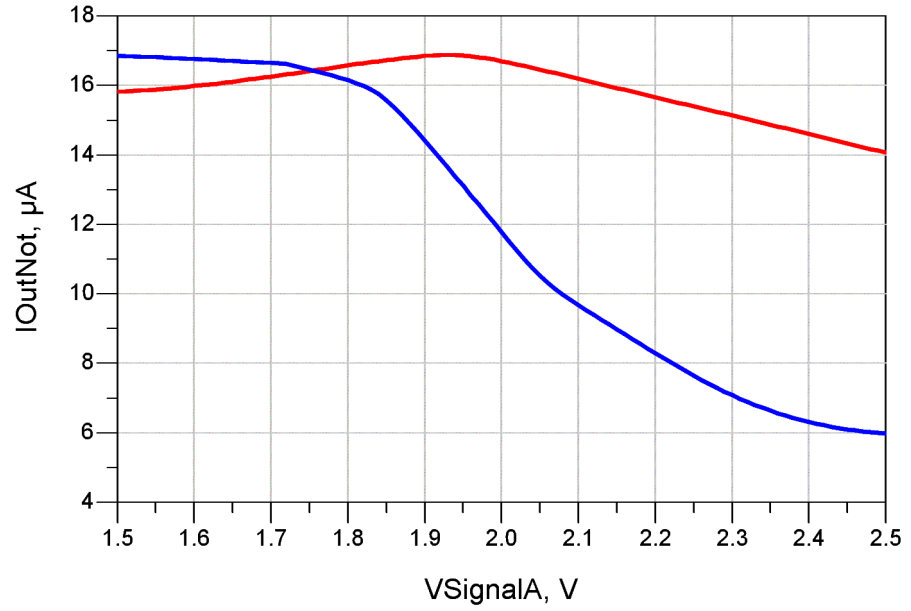

Figure 4. Current through the drain of the OutNot port versus voltage of InputA port when voltage of InputB port is low (red line) and high (blue line).

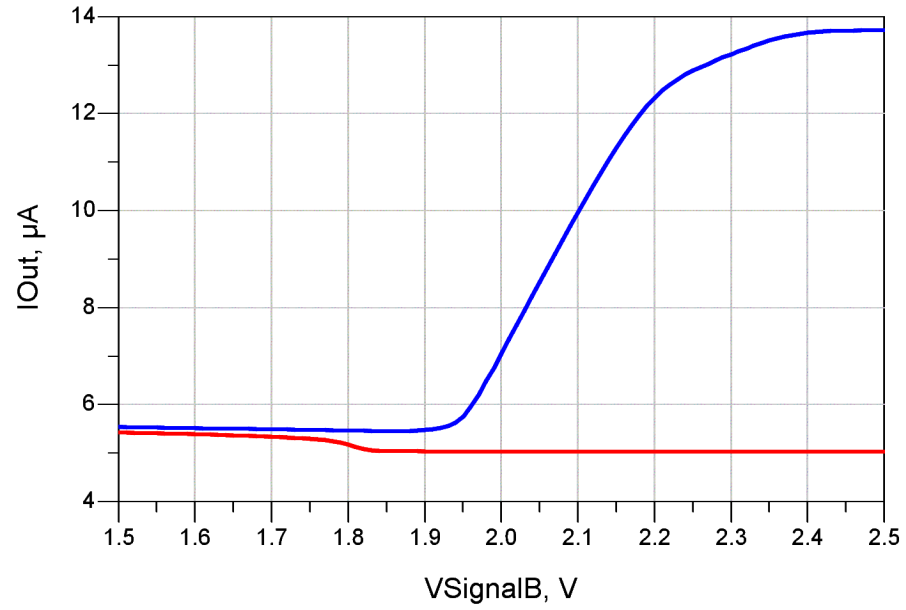

Figure 5. Current through the drain of the Out port versus voltage of InputB port when voltage of InputA port is low (red line) and high (blue line).

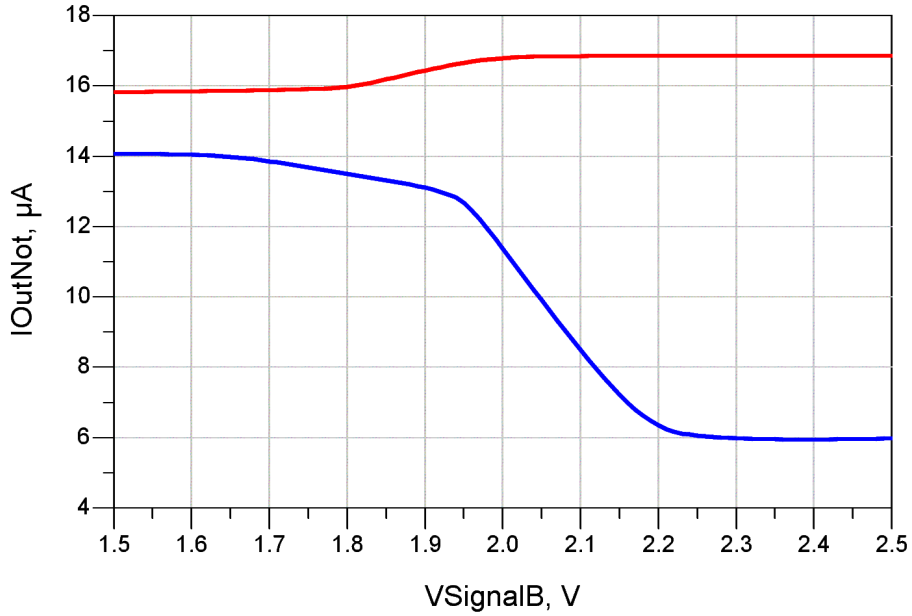

Figure 6. Current through the drain of the OutNot port versus voltage of InputB port when voltage of InputA port is low (red line) and high (blue line).

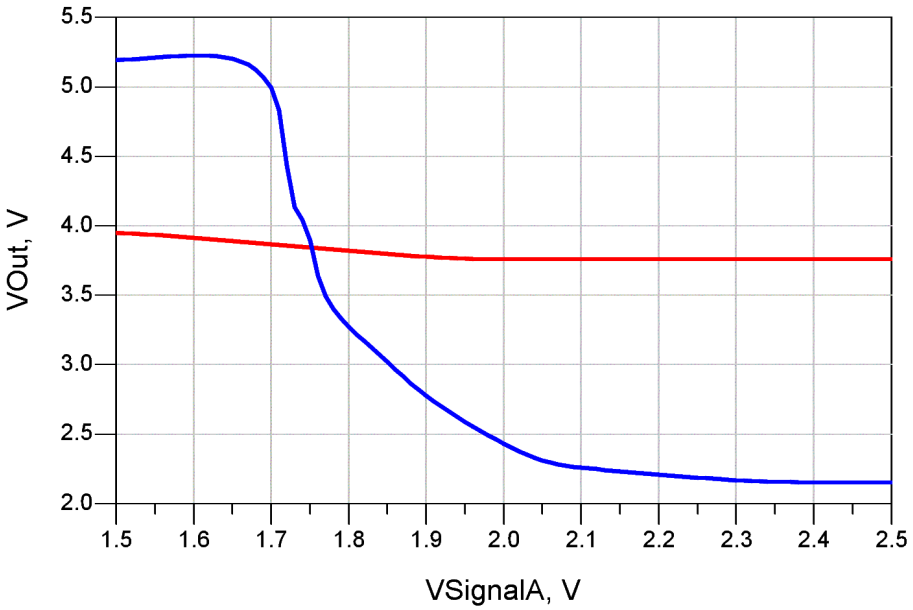

Figure 7. Voltage of the Out port versus voltage of InputA port when voltage of InputB port is low (red line) and high (blue line).

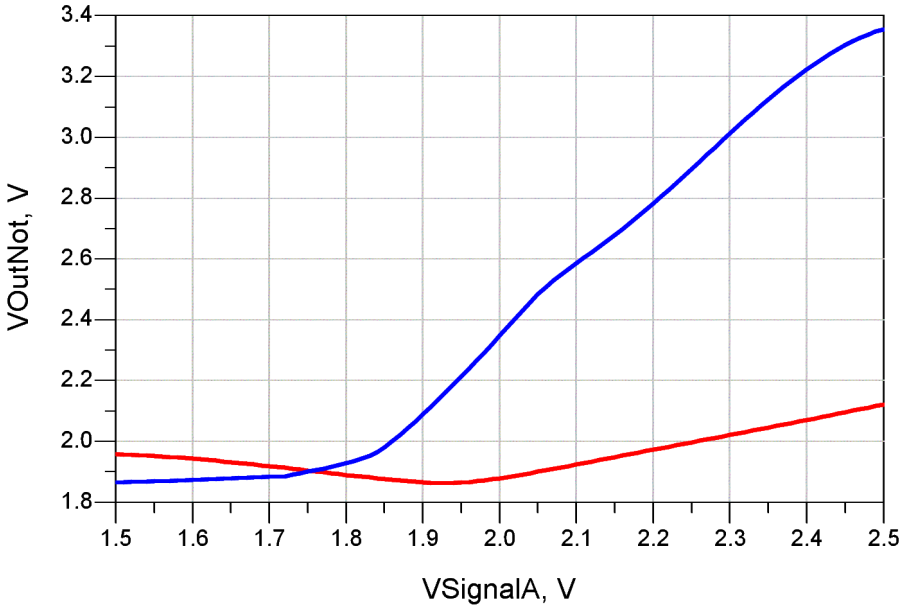

Figure 8. Voltage of the OutNot port versus voltage of InputA port when voltage of InputB port is low (red line) and high (blue line).

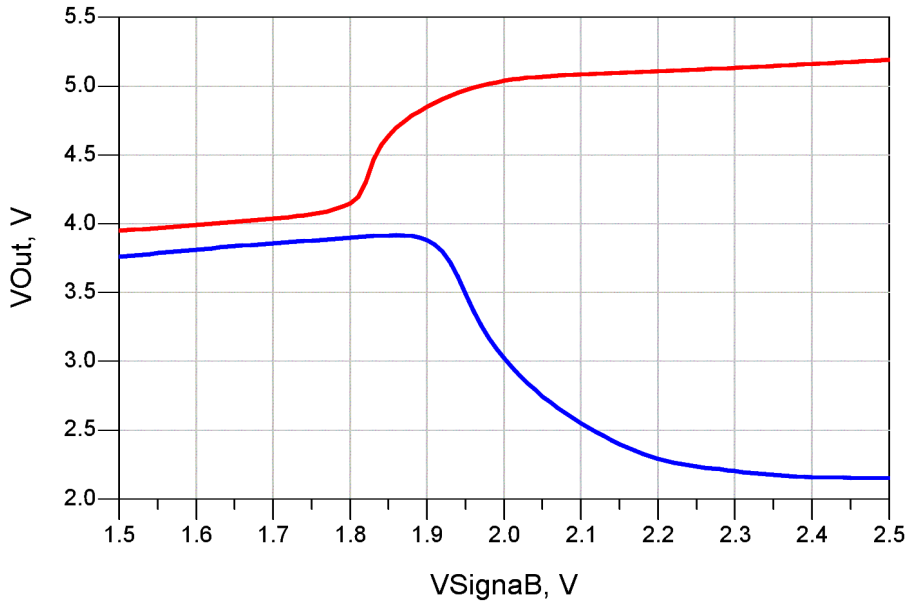

Figure 9. Voltage of the Out port versus voltage of InputB port when voltage of InputA port is low (red line) and high (blue line).

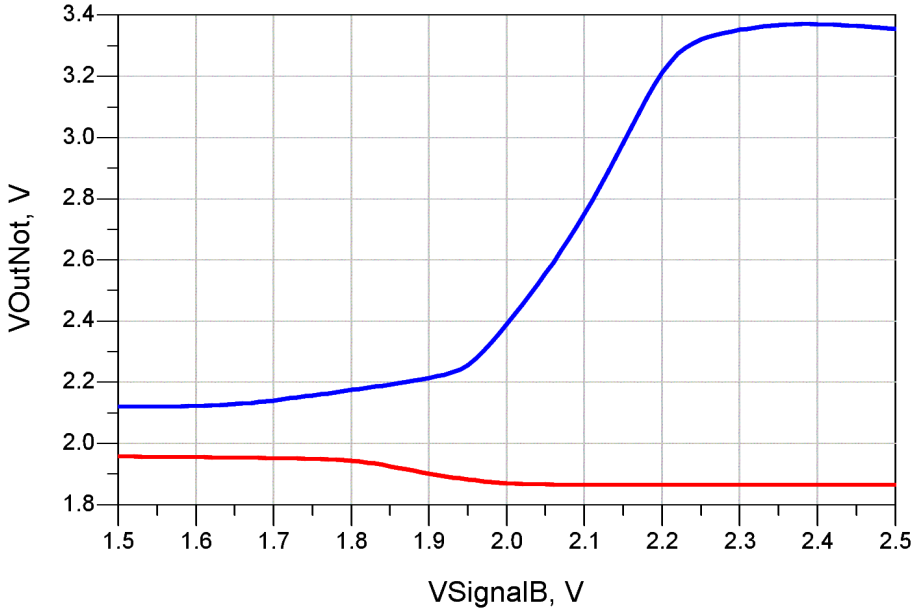

Figure 10. Voltage of the OutNot port versus voltage of InputB port when voltage of InputA port is low (red line) and high (blue line).

For voltage to voltage transfer, we need to consider separately InputA port and InputB port and for Out port and OutNot port, since all these are electrically different. Level shifters could be easily added before and after our ports, but level shifters have to be matched to the levels of the circuits attached to our ports. However, in current mode gates the preferred ports coupling is through currents not voltages. For these reasons, we do not add level shifters in this presentation.

As usual the voltage levels V_{IL}, V_{IH}, V_{OL}, V_{OH} are defined by the voltages where the differential voltage gains cross the value of 1 or −1. This level can be obtained by blue lines of Figures 7–10 representing transfer characteristics when output changes logical level.

Transfer characteristics from voltage to current do not allow clearly a definition of the point equivalent to V_{IL}, V_{IH}, V_{OL}, V_{OH} for the voltage characteristics. Indeed, while in voltage mode we can compare absolute value of the differential gain with 1 to define the aforementioned voltages. In the voltage to current characteristics, the differential gain is dimensional, and there is not an objective threshold value. Current behaviour will be clear in transient simulations.

To simplify all these values, we could unify these levels looking at the worst case.

We defined as reference voltage for input port 1.5 V for logical low and 2.5 V for logical high. These were used to fix the voltages of the not varied input port to logical low and logical high, respectively, red and blue lines, as shown in Figures 7–10.

3.2. Transient analysis

For the transient analysis we use as input the logical signal sequence (0,0) (1,0) (1,1) (0,1) (0,0) (1,1) (1,0) (0,0) (0,1) (1,1) (0,0) (1,0) (0,1) (1,0), explores all the input values and all the possible transitions.

The expected output is 0, 0, 1, 0, 0, 1, 0, 0, 0, 1, 0, 0, 0, 0 for Out port, and its negation 1, 1, 0, 1, 1, 0, 1, 1, 1, 0, 1, 1, 1, 1 for OutNot port. This signal repeats every 78 ps and has rise and fall time 1 ps. We use as input voltage values 1.5 V (low), 2.5 V (high). We used as clock frequency 180 GHz, because it is near the maximum possible, before the signal starts degrading. However, the value of 180 GHz for clock frequency is not realistic, considering the current performance of experimental CNTFETs reported in literature: this constitutes a limit to the use of CNTFET as current mode logic.

The current output in Figures 11 and 12 shows clearly a large gap between lower and higher values. Lower current (logical high) is less than 6 μA, while higher current (logical low) is all greater than 12 μA, including transient effects.

In Figure 11 we see that the current at Out port, at 68 ps, has a glitch during the transition input from (1,0) to (0,1).

In Figure 12, when we consider the current at OutNot port when the input is (1,0), at 9, 37, 64 and 75 ps, we observe that the current is lower than in the other high current output levels, but the difference is less than the separation between typical lower and higher current output.

Voltage outputs are shown in Figures 13 and 14.

We see a glitch in Figure 13, again in the Out port at 68 ps, at the same time of the glitch in current of Figure 11.

The voltage of the high logical state is not the same for all input combinations, and this is particularly clear for the output voltage of Out port.

This voltage, when the input is (0,1), is much higher than logical high output voltage for other input combinations. The difference between high output levels could be reduced adding additional CNTFETs obtaining a perfectly symmetric circuit. We avoid this solution for two reasons. First, it is fundamental to have the largest separation of voltage levels to reduce sensibility to noise, so having larger output voltage for logical state high is a benefit, not a problem. Second, adding more CNTFETs would require more chip area.

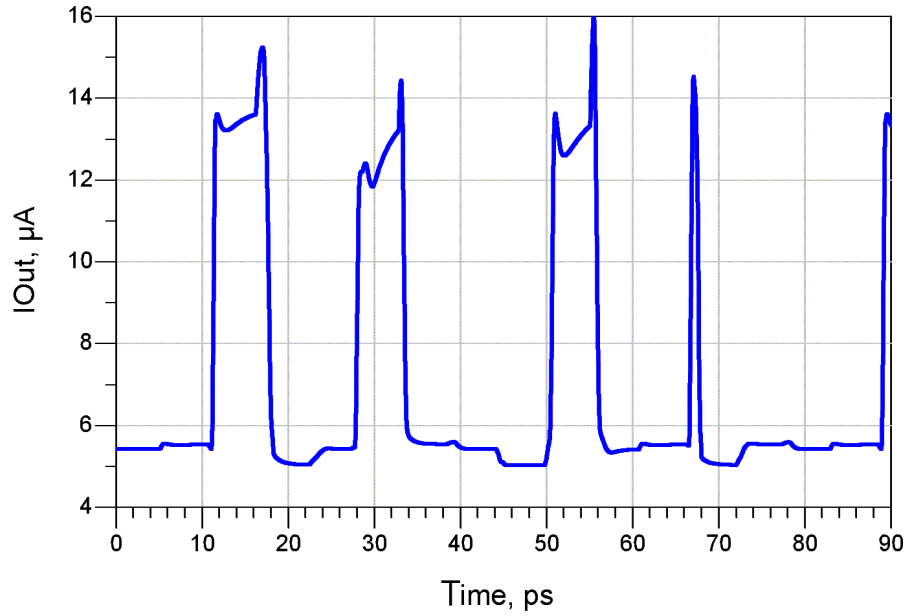

Figure 11. Current through the drain of the Out port versus time for input sequence.

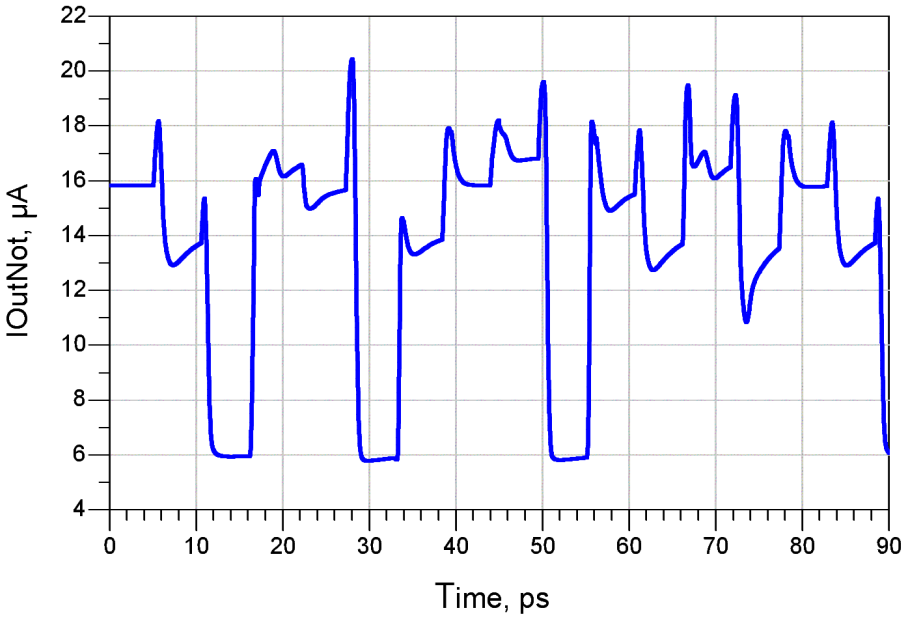

Figure 12. Current through the drain of the OutNot port versus time for input sequence.

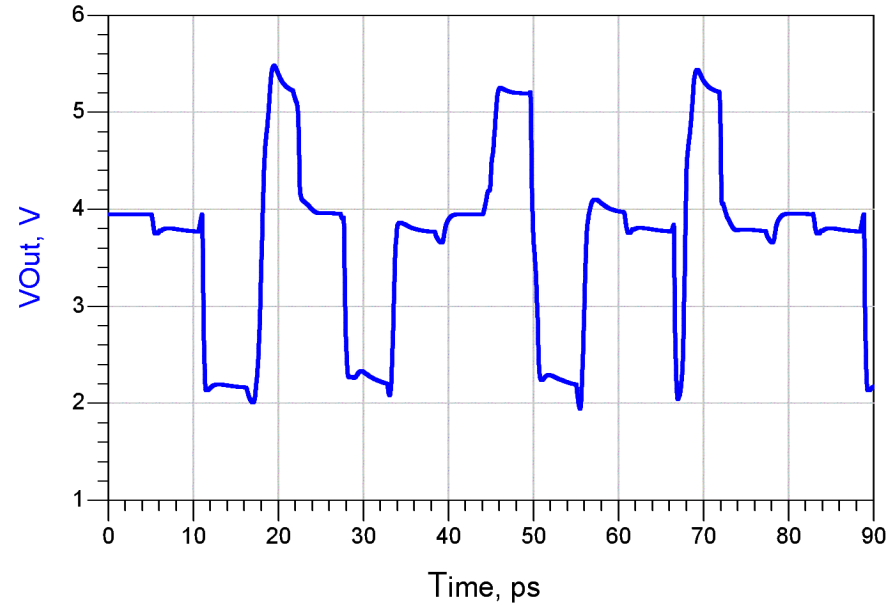

Figure 13. Voltage of the Out port versus time for input sequence.

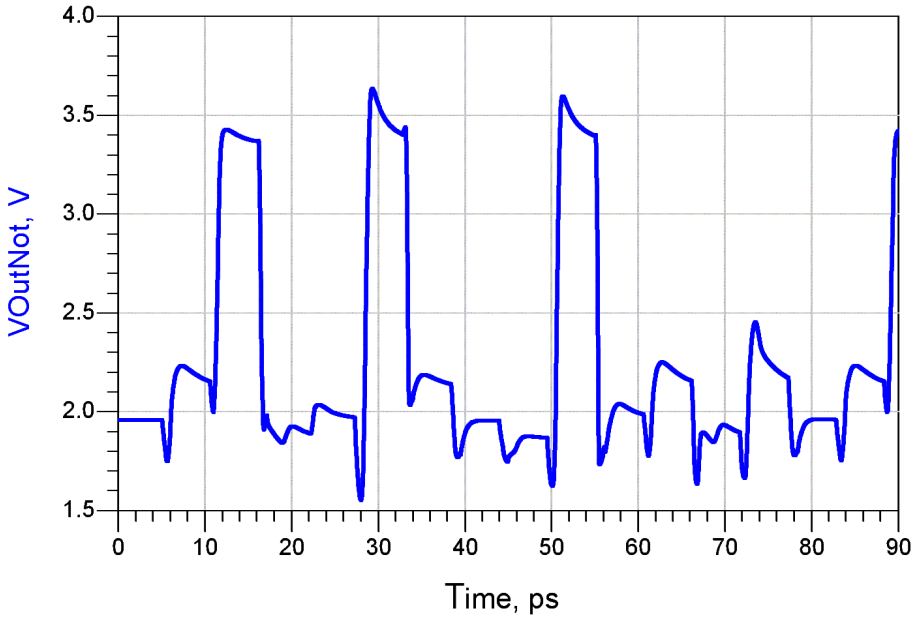

Figure 14. Voltage of the OutNot port versus time for input sequence.

The current mode logical circuit has continuous power dissipation due to the continuous current flow; therefore, the switching energy is not a specific parameter for current mode. So, we expect the power dissipation to be independent on the input data clock frequency. In energy optimized applications, this power could be reduced by external shutting down of these circuits when unused. Furthermore, chaining other gates on the same current flow reduces the total product voltage by current since voltage drop on current source and voltage drops on loads are not replicated for each port.

The instantaneous power obtained from our simulations, shown in Figure 15, as foreseen, is almost constant with some fluctuation at signal transition and just a small dependence on the input data.

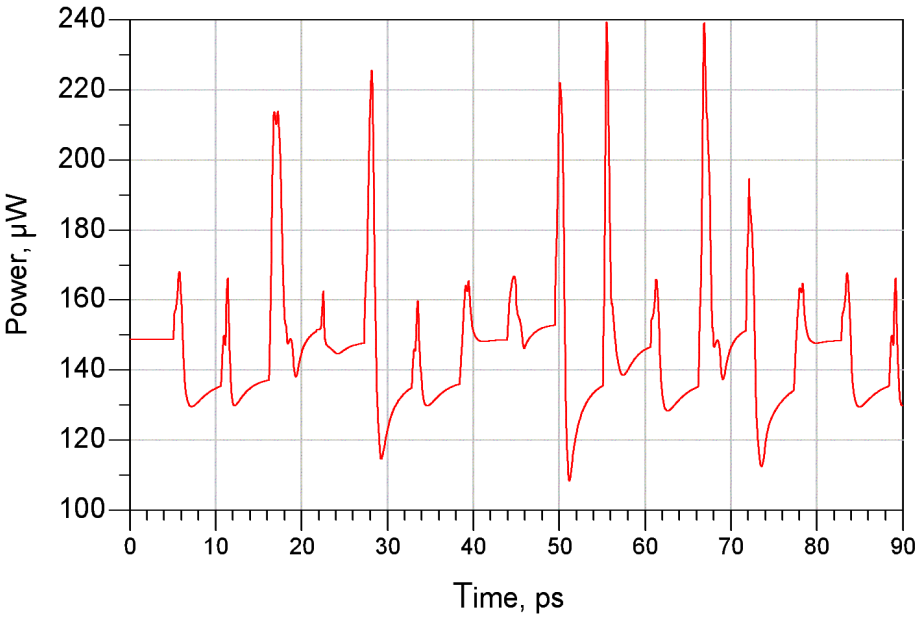

Figure 15. Instantaneous power dissipation.

The power, averaged on the presented input sequence, is 146 μW at 180 GHz. It is slightly lower at lower frequencies: for example, 145 μW at 60 GHz. This slightly lower value could come either by the simulation precision or by reduction of the contribution to the average values of the power at transient as clock periods became much larger than the transient duration.

Moreover, the obtained values of power consumption are higher than those obtained in analogous complementary metal oxide semiconductor (CMOS) circuit, demonstrating that for current mode logic, the CMOS technology is better than the CNTFET one.

For the propagation delays, we run another transient simulation where we set input rise and fall time to 0.1 ps. For the output current, the measured delay values vary depending on the input logical values and on the chosen output port. The longest value for the delay is 1.1 ps. From the measurement of the output voltage delay, again in the worst case, we obtain 1 ps.

In both the current and voltage delays, the slowest output is the Out port.

4. Conclusions

In this paper we presented a common current logical NAND/AND circuit obtained using CNTFET. Furthermore we have shown that it is possible to develop a circuit using CNTs of a single type of symmetry indices (n,m) and length.

Using CNTs with various indices or lengths would have allowed the reduction of "duplicated" CNTs, as the series X5, X7 and X6, X8 (see Figure 2), but the chip would be more problematic to realize.

The circuit could run at 180 GHz, and dissipated power is 146 μW, which is independent of clock frequency, while propagation delay is 1.1 ps. We used as clock frequency 180 GHz because it is near the maximum possible before the signal starts degrading. However, this value is not realistic considering the current performance of experimental CNTFETs, and this constitutes a limit to the use of CNTFETs as current mode logic. Moreover, the obtained values of power consumption are higher

than those obtained in analogous CMOS circuit, demonstrating that for current mode logic, the CMOS technology is better than the CNTFET one.

More current mode gates could be chained by adding differential pairs along the current path, but voltage levels must be carefully chosen, and level shifter must be added at input and output of the chain of current mode ports.

We are now investigating how to make delay time shorter, and we intend to repeat the proposed simulations using other CNTFET models, such the model proposed in [31,32], in order to have comparable results.

Currently, we are also working to study the effect of noise [33] in other circuits based on CNTFETs. Moreover, we are analyzing more thoroughly the effects of parasitic elements of interconnection lines in CNT embedded integrated circuits [34] and the impact of technology on CNTFET-based circuit performance [35].

Use of AI tools declaration

The authors declare they have not used Artificial Intelligence (AI) tools in the creation of this article.

Conflict of interest

The authors declare no conflict of interest.

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