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Research article

Analysis of temperature dependent power supply voltage drop in graphene nanoribbon and Cu based power interconnects

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Abstract: In this paper, we propose a temperature dependent resistive model of multi layered graphene nanoribbon (MLGNR) and Cu based power interconnects. Using the proposed model, power supply voltage drop (IR-drop) analysis for 16 nm technology node is performed. The novelty in our work is that this is the first time a temperature dependent IR-Drop model for MLGNR and Cu interconnects is proposed. For a temperature range from 150 K to 450 K, the variation of resistance of MLGNR interconnect is ~2–5× times lesser than that of traditional copper based power interconnects. Our analysis shows that MLGNR based power interconnects can achieve ~1.5–3.5× reduction in IR-drop and ~1.5–3× reduction in propagation delay as compared with copper based interconnects for local, intermediate and global interconnects.

Keywords: temperature; graphene nanoribbon (GNR); interconnects; power supply voltage drop (IR-drop); mean free path (MFP); international technology roadmap for semiconductors (ITRS)

1. Introduction

Power supply voltage drop (IR-drop) has been one of most important challenges of power interconnects in sub nanometer designs [1–4]. It becomes even more challenging for the high density and high performance designs in which it has adverse effects on timing. The increase in chip operating temperature has two-fold effects on timing. Firstly, it increases the interconnect resistance which in turn increases the interconnect delay. Secondly, due to the increase in resistance there is more IR-drop which also increases the gate delay. Therefore, it is very essential to analyze the effects of temperature on IR-drop in sub nanometer designs, since the resistivity of the traditional copper based interconnects increases significantly in nanometer dimensions [5]. GNR is one of the most promising material for interconnect modeling for future generation technologies [5,6] due to its excellent properties compared with copper in nanometer dimensions. Recent studies [6–10] on GNR show its superiority over the traditional copper based interconnects. The compact resistance modeling with only absolute temperature (300 K) in MLGNR stacks is proposed by Sansiri Tanachutiwat et al. reported in [11]. The temperature independent IR-Drop induced delay-fault model and simultaneous switching noise for MLGNR interconnects has been investigated by D. Das et al. reported in [12,13,14]. The temperature dependent comparisons of delay between CNT and Cu have been investigated in [15,16]. However, as per our knowledge no investigation has been carried out to analyze the effects of the temperature on IR-drop in multi layer graphene nanoribbon (MLGNR) interconnect till date. Motivated by the previous work, we have proposed a temperature dependent resistive model of multi layer graphene nanoribbon (MLGNR) interconnect. Using the proposed model, we have analyzed the power supply voltage drop (IR-drop) and delay in MLGNR based power interconnects. The rest of the paper is organized as follows. Section 2 and 3 presents the proposed temperature dependent resistive model of MLGNR and Cu interconnect. The results and conclusions are presented in the Sections 4 and 5.

2. Temperature Dependent Resistance Model of MLGNR Interconnect

A multilayer GNR (MLGNR) structure is shown in Figure 1 is used for modeling power interconnects in nanoscale design. The width, thickness, and height of the MLGNR structure are denoted by w, t, and ht, respectively. The separation between two MLGNR structures is denoted by sp. In our interconnect design, we have considered width (w) = 16 nm and thickness (t) = 32 nm for 16 nm International technology roadmap for semiconductors (ITRS) technology node [5]. The total number of SLGNR present in proposed MLGNR structure is given by [7].

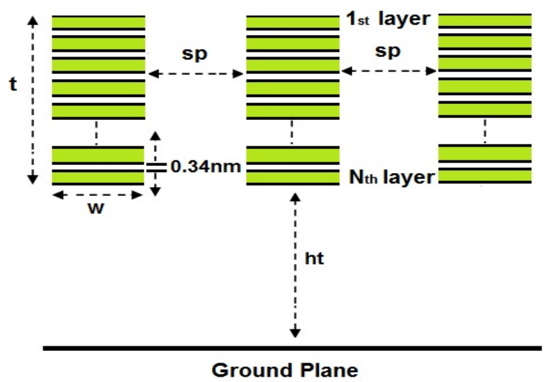

Figure1. Schematic representation of multi-layer GNR interconnect.

$$N_{layer} = 1 + Integer\,[t/\delta] \tag{1}$$

The interlayer spacing (δ) between two consecutive graphene layers is 0.34 nm which is called as van der walls gap. Using (1) we obtain the total number of SLGNR present in proposed MLGNR structure as N_{layer} = 95 for 16 nm technology node. The total resistance of MLGNR is given by.

$$R_{Total-MLGNR} = R_Q(1+\frac{l_{MLGNR}}{\lambda_{effective}})+R_c \quad (2)$$

where l_{MLGNR} is the length of MLGNR based interconnect and $\lambda_{effective}$ is the effective electron mean free path (MFP) of MLGNR. The quantum resistance (R_Q) of SLGNR is 12.94 kΩ. The contact resistance is assumed as 100 Ω·µm. The quantum resistance for MLGNR expressed as [7]

$$R_Q = \frac{h/2.e^2}{N_{ch}.N_{layer}} = \frac{12.94\ k\Omega}{N_{ch}.N_{layer}} \quad (3)$$

In (3) N_{ch} is the number of conducting channels in SLGNR, N_{layer} is the number of layer present in MLGNR, h is the Planck's constant, and e is the electronic charge. The number of conducting channel present in SLGNR is given by [8,10]

$$N_{ch} = \sum_{j=1}^{n_C}[1+e^{(E_{j,n}-E_F)/k_BT}]^{-1} + \sum_{j=1}^{n_V}[1+e^{(E_F+E_{j,h})/k_BT}]^{-1} \quad (4)$$

where $j = (1, 2, 3, \ldots)$ is a positive integer, E_F is Fermi energy, k_B is the Boltzmann's constant, T is temperature, and n_c and n_v are the number of conduction and valance sub-bands. $E_{j,n}$ and $E_{j,h}$ are the minimum energy of electron and hole in j_{th} conduction sub-band as given by [8]

$$E_j = \Delta E\left|j+\beta\right| \text{ , where } \Delta E = \frac{hv_f}{2w} \quad (5)$$

ΔE is the sub-band energy in metallic GNR and β value is zero for metallic GNR and it is 1/3 in semiconducting GNR [8,10]. The Fermi potential for metallic GNR has been consider between 0.21 eV to 0.4 eV reported in [8,10]. The Fermi potential may varies in stacked multilayered GNR in each layer. Therefore, the value of Fermi energy for the inner layer GNR is derived as [11].

$$E_{F,m} = E_F e^{-\delta m/\Psi} \quad (6)$$

In (6), "m" is the position of the layer in stacked MLGNR structure, $\delta = 0.34$ nm and $\Psi = 0.387$ nm is the fitting parameter reported in [11]. The average of all Fermi potential for top, bottom and inner layers (total Nlayer ≅ 95) is equal to 0.3 eV. The number of conducting channels (N_{ch}) is 6 for metallic SLGNR of width 16 nm for $E_F = 0.3$ eV. The effective MFP of SLGNR interconnects depends on three important parameters: electron-electron scattering (λ_e), acoustic phonon scattering (λ_{ap}) and remote interfacial phonon scattering (λ_{rip}). Electron-electron scattering independent with temperature variation, but remaining two parameters vary with temperature which adversely affects on the interconnect delay due to change in resistance followed by temperature variation. The electron-electron scattering λ_e can be expressed as [11]

$$\lambda_e = \lambda_{defect} + w\sum_{i=1}^{N_{ch}}\sqrt{\frac{N_{ch}}{i}-1} \quad (7)$$

where, λ_{defect} is the MFP of SLGNR due to the defects exists inside the graphene layer. Here, "*i*" is an integer variable which varies from 1 to N_{ch} = 6 and "*w*" is the interconnect width of MLGNR interconnect. The value of λ_{defect} is assumed to be 1 µm [11]. The MFP due to acoustic phonon scattering λ_{ap} can be expressed as [11]

$$\lambda_{ap} = \frac{h^2 \rho_s v_s^2 v_f^2 w}{\pi^2 D_A^2 k_B T} \tag{8}$$

In (8), v_f is the Fermi velocity of GNR (= 8 × 10^5 m/s), v_s is the sound velocity of GNR (= 2.1 × 10^4 m/s), D_A is the acoustic deformation potential, k_B is the Boltzmann constant, ρ_s is the 2D mass density of graphene, and T is the temperature. The MFP due to remote interfacial phonon scattering λ_{rip} is expressed as [11]

$$\lambda_{rip} = \alpha E_F^{1.02} w \left(e^{\frac{E_0}{kT}} - 1\right) \tag{9}$$

where α is the fitting parameter, E_F is the Fermi potential, and E_0 = 104 mV. The temperature dependent effective MFP of SLGNR is given by applying Matthiessen's rule [11]

$$\lambda_{effective} = \left[(\lambda_e)^{-1} + (\lambda_{ap})^{-1} + (\lambda_{rip})^{-1}\right]^{-1} \tag{10}$$

The values of λ_e, λ_{ap}, λ_{rip}, *and* $\lambda_{effective}$, for different temperature are shown in Figure 2. Substituting the effective MFP of SLGNR in (2) we obtain the temperature dependent resistance of MLGNR in (11). The temperature dependent resistance values for different length and different temperatures for GNR interconnect is shown in Figure 3.

$$R_{Total-MLGNR} = R_Q\left[1 + \frac{l_{MLGNR}(\lambda_e\lambda_{ap} + \lambda_{ap}\lambda_{rip} + \lambda_{rip}\lambda_e)}{(\lambda_e\lambda_{ap}\lambda_{rip})}\right] \tag{11}$$

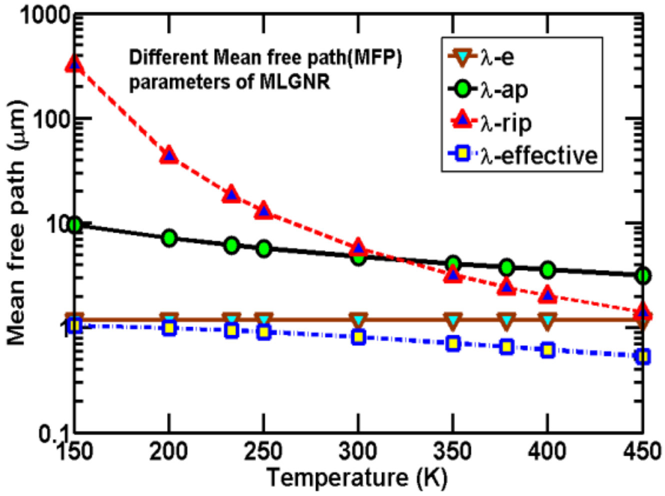

Figure 2. Different MFP vs. temperature of multi-layer GNR interconnects.

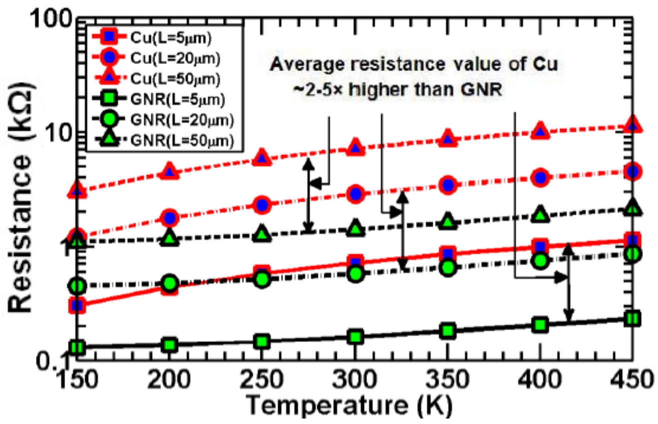

Figure 3. Resistance vs. temperature plot for GNR and Cu interconnects 16 nm technology.

3. Temperature Dependent Resistance Model of Cu Interconnect

The temperature dependent resistive model of Cu based nanointerconnect is explained in this section. To implement this model, surface roughness scattering and grain boundary scattering phenomena are considered. The surface roughness scattering based resistivity model first proposed by Fuchs [17] and Sondheim [18] (FS-model) which is given by (12)

$$\frac{\rho_{FS}}{\rho_O} = 1 + \frac{3}{4}\frac{\lambda_O}{w}(1 - P) \tag{12}$$

where ρ_o is the resistivity of the bulk material, w is width of the nanointerconnect, λ_o is the mean free path of the conduction electrons, and P (= 0.6) is the Fuchs scattering parameter. The grain boundary scattering based resistivity model is proposed by Mayadas and Shatzkes (MS-model) [19] which is given by (13)

$$\frac{\rho_{MS}}{\rho_O} = \left[1 - \frac{3}{2}\alpha + 3\alpha^2 - 3\alpha^3 \ln(1 + \frac{1}{\alpha})\right]^{-1} \tag{13}$$

$$\text{Where, } \alpha = \frac{\lambda_O}{D}(\frac{R}{1 - P})$$

Here D is the mean grain size and R is the reflection coefficient in the grain edges or boundaries with values in between 0 and 1. In our model, we have considered the mean grain size is equivalent to film width and R = 0.33. The total resistivity of Cu nanointerconnect can be measured by combined effects of surface roughness and grain boundary scattering as given in (14)

$$\rho_{Cu} = \rho_{FS} + \rho_{MS} \tag{14}$$

In (14) we have shown the temperature independent resistivity of Cu nanointerconnect. In general, the electrical resistivity of Cu nanointerconnects increases with temperature due to electron-phonon interactions mechanism [20]. As the temperature increase linearly, the resistance of Cu nanointerconnect also increases linearly. For Cu nanointerconnects, the temperature dependent resistivity $\rho_{cu}(T)$ follows a power law function of temperature which is given by the Bloch-Grüneisen model given in (15) [20,21,22]

$$\rho_{Cu}(T) = \rho_{Cu}(0) + 4R(\Theta_R)\left[\frac{T}{\Theta_R}\right]^n \int_0^{\frac{\Theta_R}{T}} \frac{x^n}{(e^x-1)(1-e^{-x})}dx \tag{15}$$

Here, $R(\Theta_R) = \frac{\eta}{e^2}\left[\frac{\pi^3(3\pi^2)^{1/3}\eta^2}{4n_{cell}^{2/3}aMk_B\Theta_R}\right]$

Θ_R, is the Debye temperature used for resistivity calculation of Cu interconnect in nanometer dimension [20,21,22]. The Debye temperature Θ_R, is taken ~320 K for bulk non-magnetic material like Cu [22]. In our analysis, the residual resistivity $\rho_{Cu}(0)$ in (15) has been ignored because it is temperature independent parameter and occurs due to presence of defect scattering [22]. Here η = Planck's constant divided by *2π*, n_{cell} = number of electron's present in an atom which participate in current conduction, the atomic mass M = (atomic weight)/N_A, where N_A is the Avogadro's number, a = $(\text{volume/atom})^{1/3}$, k_B is Boltzmann's constant, and *e* is the electron charge. Here "*n*" is an integer which depends on the characteristics of interaction. In general the value of "*n*" lies between 2–5.

1. n = 5 signifies that the resistance variation is due to scattering of electrons by phonons (for simple metals like Cu) [23];
2. n = 3 signifies that the resistance variation is due to s-d (spin density) electron scattering (for transition metals or dilute alloys) [23];
3. n = 2 signifies that the resistance variation is due to electron-electron collisions or interaction. [23];

In our analysis we have considered the 1st condition. Thus, the temperature dependent resistance of Cu nanointerconnect is given by (16)

$$R_{Cu}(T) = \rho_{Cu}(T).\frac{l}{wt} \tag{16}$$

where *l* = length, *w* = width, and *t* = thickness of Cu nanointerconnect. Here "*w*" is 16 nm and "*t*" is 32 nm for 16 nm ITRS technology node for Cu interconnect same as MLGNR interconnect. Length of Cu nanointerconnect is varied from 10 µm to 100 µm. The temperature dependent resistance values of Cu nanointerconnect for different lengths at different temperature are shown in Figure 3.

4. Results

Using the temperature dependent resistance model as discussed in previous section, we have calculated the resistance for different interconnect length and different temperature. In Figure 3 we have shown the temperature dependent resistance of MLGNR and Cu interconnect for different interconnect length (5 µm to 50 µm) for 16 nm technology node. MLGNR shows ~2–5× less resistance than that of Cu as shown in Figure 3. In Figure 2, with the increase in temperature, the effective mean free path reduces, and hence the scattering induced ohomic part of the total resistance of MLGNR increases. The IR-drop analysis is performed in MLGNR and Cu interconnects for 5 µm (local), 20 µm (intermediate) and 50 µm (global) interconnect lengths. The analysis is performed using equivalent circuit model shown in Figure 4.

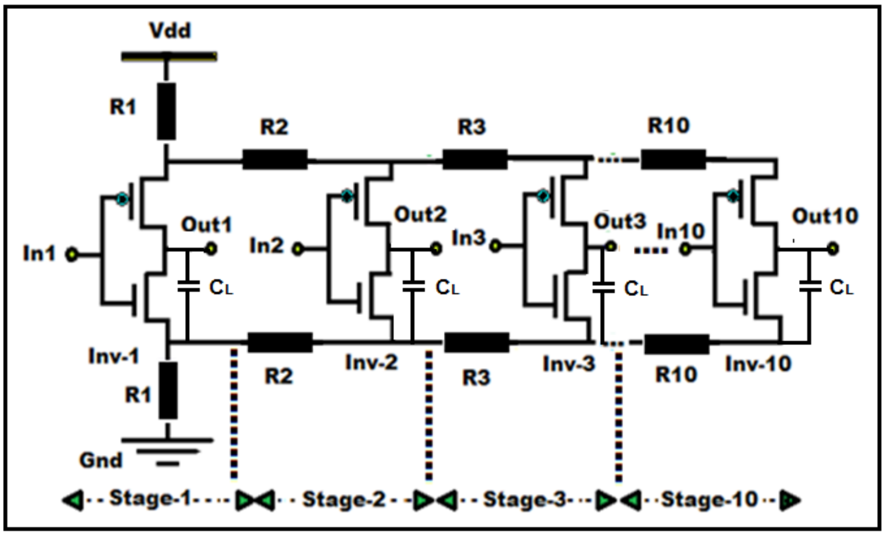

Figure 4. Schematic circuit used for power supply voltage drop analysis.

In Figure 4, ten identical CMOS inverters are connected in series with temperature dependent resistance for both MLGNR and Cu. In our analysis, we have assumed the supply voltage as 0.7 V, the input voltage swing is from 0 to 0.7 V for all stages and pulse rise/fall time is assumed as 100 ps. The CMOS inverters are designed for 16 nm ITRS technology node using the SPICE models from predictive technology model [24]. MOSFET model parameters are defined in Table 1. The simulations are performed using the Cadence spectra simulator. All the inverters are switched simultaneously so that they draw current from the power supply. As a result the power supply voltage decreases progressively away from the power pad. The decrease in power supply causes increase in propagation delay through the gate. As the temperature increases, the resistance of the power interconnects increases which causes more interconnect delay. With temperature as the IR-drop increases, the gates suffer more delay problem. Therefore, increase in temperature has twofold increase in delay: one due to increase in interconnect (RC) delay and the other due to increase in IR-drop. Figure 5–7 illustrate the IR-drop in GNR and Cu interconnects for local, intermediate, and global lengths. It is observed that the IR-drop increases with the increase in temperature both for MLGNR and Cu interconnects but MLGNR shows ~1.5–3.5× less IR-drop than Cu at local, intermediate and global lengths. The IR-Drop analyzed data shown in Table 2, Table 3 and Table 4, where maximum, minimum and average IR-Drop of MLGNR and Cu interconnects are present. The total propagation delay of MLGNR and Cu interconnect shown in Table 5. In our analysis, we also find out that MLGNR interconnect can reduce delay up to ~1.5–3× compared with Cu interconnect.

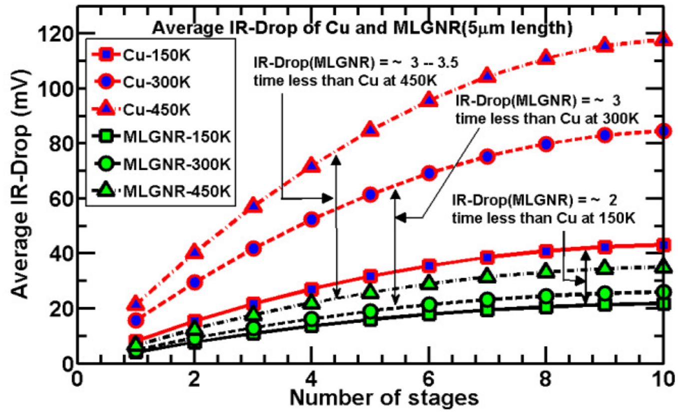

Figure 5. Average IR-drop vs. No of Stages of Cu and MLGNR interconnect at different temperature for 5 μm length (local level).

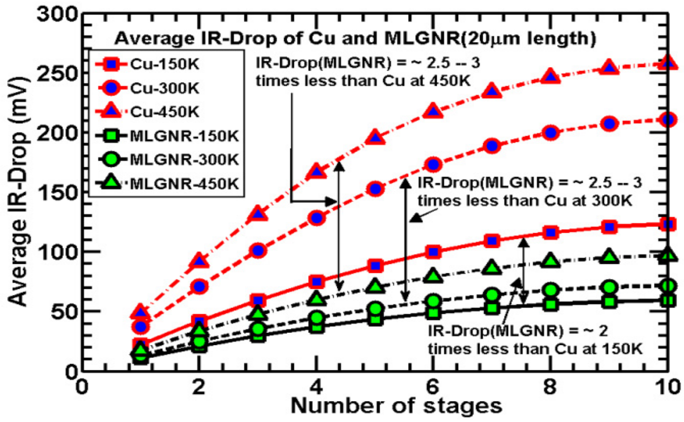

Figure 6. Average IR-drop vs. No of Stages of Cu and MLGNR interconnect at different temperature for 20 μm length (intermediate level).

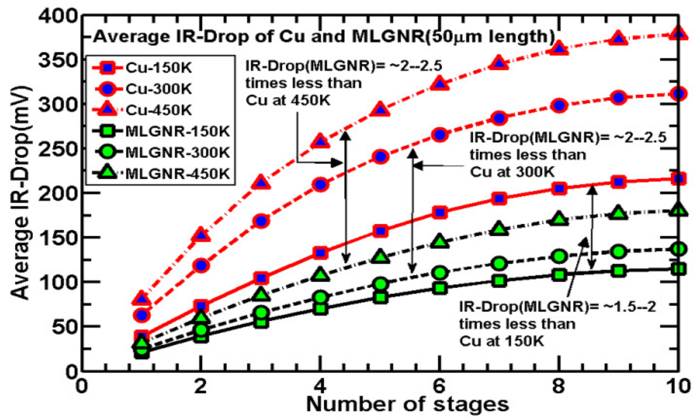

Figure 7. Average IR-drop vs. No of Stages of Cu and MLGNR interconnect at different temperature for 50 μm length (global level).

Table 1. 16 nm Predictive Technology Model (PTM) CMOS Model Parameter.

Model Parameters [24]	n-MOS(Si)	p-MOS(Si)
Channel Length (L)	16 nm	
Channel Width (W)	64 nm	128 nm
Threshold Voltage (V_{TH0})	0.47 volt	−0.43 volt
Dielectric Constant (ε_{ox} for Sio_2)	$\varepsilon_{ox} = 3.9 \times \varepsilon_0$,Where $\varepsilon_0 = 8.85 \times 10^{-12}$ F/m	
Oxide Thickness(t_{ox})	0.95 nm	1 nm
Gate Oxide Capacitance (C_{ox})	0.29 fF	0.28 fF
Junction Depth (X_j)	5 nm	

Table 2. Temperature dependent IR-Drop (mV) of MLGNR and Cu interconnect for 16 nm technology and 5 µm length (local length).

Temperature (K)→	150	200	250	300	350	400	450	150	200	250	300	350	400	450
No of Stages ↓	Maximum Peak IR-Drop of MLGNR							Maximum Peak IR-Drop of Cu						
1st	7.04	7.32	7.76	8.40	9.23	10.20	11.30	13.81	18.41	22.46	26.08	29.34	32.33	35.10
2nd	13.25	13.77	14.60	15.79	17.34	19.16	21.21	25.92	34.55	42.17	48.97	55.11	60.77	65.93
3rd	18.68	19.41	20.57	22.25	24.41	26.98	29.86	36.47	48.64	59.41	69.05	77.82	85.88	93.29
4th	23.36	24.28	25.72	27.81	30.52	33.72	37.31	45.60	60.87	74.43	86.61	97.72	107.94	117.41
5th	27.33	28.39	30.09	32.52	35.70	39.43	43.63	53.34	71.25	87.24	101.70	114.88	127.04	138.35
6th	30.61	31.80	33.69	36.41	39.96	44.15	48.86	59.72	79.87	97.93	114.25	129.29	143.18	156.11
7th	33.21	34.51	36.56	39.51	43.35	47.90	53.02	64.83	86.78	106.46	124.45	140.87	156.21	170.55
8th	35.15	36.53	38.69	41.82	45.88	50.69	56.11	68.64	91.94	112.94	132.03	149.76	166.17	181.48
9th	36.45	37.87	40.11	43.35	47.56	52.55	58.17	71.18	95.37	117.25	137.19	155.68	172.75	188.97
10th	37.09	38.54	40.82	44.12	48.40	53.47	59.20	72.44	97.07	119.39	139.79	158.62	176.19	192.74
No of Stages	Minimum Peak IR-Drop of MLGNR							Minimum Peak IR-Drop of Cu						
1st	1.18	1.23	1.31	1.43	1.59	1.79	2.02	2.55	3.54	4.47	5.36	6.19	6.98	7.74
2nd	2.24	2.33	2.49	2.71	3.02	3.40	3.83	4.84	6.72	8.49	10.18	11.75	13.27	14.73
3rd	3.17	3.31	3.53	3.85	4.30	4.83	5.44	6.87	9.55	12.07	14.45	16.69	18.88	20.93
4th	3.99	4.16	4.44	4.85	5.41	6.08	6.85	8.64	12.03	15.20	18.18	21.05	23.78	26.42
5th	4.69	4.89	5.21	5.71	6.36	7.15	8.06	10.15	14.15	17.89	21.37	24.79	27.97	31.15
6th	5.27	5.50	5.86	6.42	7.16	8.04	9.06	11.41	15.91	20.12	24.07	27.89	31.54	35.09
7th	5.73	5.98	6.38	6.99	7.80	8.75	9.86	12.42	17.32	21.91	26.23	30.37	34.39	38.23
8th	6.08	6.34	6.77	7.42	8.27	9.28	10.46	13.17	18.37	23.25	27.85	32.23	36.53	40.59
9th	6.31	6.58	7.03	7.71	8.59	9.64	10.86	13.67	19.08	24.14	28.93	33.47	37.96	42.21
10th	6.43	6.70	7.16	7.85	8.75	9.82	11.06	13.92	19.43	24.59	29.47	34.09	38.67	43.02
No of Stages	Average IR-Drop of MLGNR							Average IR-Drop of Cu						
1st	4.11	4.27	4.53	4.91	5.41	5.99	6.66	8.18	10.97	13.46	15.72	17.76	19.65	21.42
2nd	7.74	8.05	8.54	9.25	10.18	11.28	12.52	15.38	20.63	25.33	29.57	33.43	37.02	40.33
3rd	10.92	11.36	12.05	13.05	14.35	15.90	17.65	21.67	29.09	35.74	41.75	47.25	52.38	57.11
4th	13.67	14.22	15.08	16.33	17.96	19.90	22.08	27.12	36.45	44.81	52.39	59.38	65.86	71.91
5th	16.01	16.64	17.65	19.11	21.03	23.29	25.84	31.74	42.70	52.56	61.53	69.83	77.50	84.75
6th	17.94	18.00	19.77	21.41	23.56	26.09	28.96	35.56	47.89	59.02	69.16	78.59	87.36	95.60

7th	19.47	20.24	21.47	23.25	25.57	28.32	31.44	38.62	52.05	64.18	75.34	85.62	95.30	104.39
8th	20.61	21.43	22.73	24.62	27.07	29.98	33.28	40.90	55.15	68.09	79.94	90.99	101.35	111.03
9th	21.38	22.22	23.57	25.53	28.07	31.09	34.51	42.42	57.22	70.69	83.06	94.57	105.35	115.59
10th	21.76	22.62	23.99	25.98	28.57	31.64	35.13	43.18	58.25	71.99	84.63	96.35	107.43	117.88

Table 3. Temperature dependent IR-Drop (mV) of MLGNR and Cu interconnect for 16 nm technology and 20 µm length (intermediate length).

Temperature (K)→	150	200	250	300	350	400	450	150	200	250	300	350	400	450
No of Stages ↓	Maximum Peak IR-Drop of MLGNR							Maximum Peak IR-Drop of Cu						
1st	18.76	19.53	20.73	22.42	24.54	26.98	29.550	36.53	45.66	53.24	59.90	65.91	71.52	76.76
2nd	35.22	36.66	38.89	42.10	46.08	50.67	55.50	68.66	85.83	100.02	112.40	123.57	133.86	143.45
3rd	49.57	51.63	54.82	59.30	65.01	71.49	78.38	97.18	121.74	142.15	159.91	175.86	190.47	204.12
4th	62.05	64.60	68.60	74.29	81.48	89.63	98.43	122.30	153.86	180.08	202.92	223.39	241.75	257.80
5th	72.62	75.66	80.40	87.08	95.52	105.27	115.73	144.25	182.19	213.81	241.34	264.33	283.27	299.31
6th	81.45	84.87	90.14	97.75	107.38	118.40	130.28	162.87	206.46	242.96	272.94	295.93	314.48	329.98
7th	88.49	92.17	98.03	106.25	116.77	128.87	141.92	178.00	226.45	266.87	296.76	319.25	337.19	352.06
8th	93.74	97.68	103.9	112.73	123.96	136.91	150.92	189.68	241.95	284.23	313.66	335.60	352.97	367.26
9th	97.23	101.3	107.8	117.03	128.75	142.26	156.87	197.40	252.44	295.44	324.46	345.97	362.91	376.79
10th	98.96	103.2	109.7	119.17	131.14	144.92	159.82	201.38	257.80	300.94	329.72	351.00	367.71	381.38
No of Stages	Minimum Peak IR-Drop of MLGNR							Minimum Peak IR-Drop of Cu						
1st	3.62	3.79	4.07	4.46	4.98	5.59	6.25	8.15	10.90	13.29	15.45	17.43	19.22	20.86
2nd	6.87	7.20	7.72	8.47	9.46	10.61	11.85	15.50	20.74	25.42	29.68	33.56	37.11	40.50
3rd	9.77	10.23	10.96	12.04	13.44	15.05	16.85	22.07	29.65	36.45	42.66	48.41	53.75	58.81
4th	12.30	12.88	13.79	15.17	16.92	18.93	21.24	27.86	37.47	46.25	54.35	61.91	69.05	75.84
5th	14.46	15.14	16.24	17.85	19.89	22.30	25.01	32.82	44.33	54.86	64.64	73.97	82.82	91.31
6th	16.26	17.02	18.28	20.08	22.37	25.11	28.14	36.95	50.10	62.19	73.58	84.38	94.85	104.92
7th	17.70	18.53	19.91	21.86	24.34	27.36	30.64	40.33	54.70	68.18	80.88	93.07	104.88	116.36
8th	18.78	19.67	21.13	23.20	25.83	29.05	32.52	42.89	58.29	72.67	86.50	99.77	112.64	125.29
9th	19.49	20.43	21.94	24.09	26.83	30.17	33.76	44.59	60.69	75.80	90.24	104.33	118.00	131.35
10th	19.85	20.81	22.35	24.53	27.34	30.73	34.40	45.44	61.89	77.37	92.19	106.61	120.72	134.47
No of Stages	Average IR-Drop of MLGNR							Average IR-Drop of Cu						
1st	11.19	11.66	12.40	13.44	14.76	16.28	17.90	22.34	28.28	33.26	37.67	41.67	45.37	48.81
2nd	21.04	21.93	23.30	25.28	27.77	30.64	33.67	42.08	53.28	62.72	71.04	78.56	85.48	91.97
3rd	29.67	30.93	32.89	35.67	39.22	43.27	47.61	59.62	75.69	89.30	101.28	112.13	122.11	131.46
4th	37.17	38.74	41.19	44.73	49.20	54.28	59.83	75.08	95.66	113.16	128.63	142.65	155.40	166.82
5th	43.54	45.40	48.32	52.46	57.70	63.78	70.37	88.53	113.26	134.33	152.99	169.15	183.04	195.31
6th	48.85	50.94	54.21	58.91	64.87	71.75	79.21	99.91	128.28	152.57	173.26	190.15	204.66	217.45
7th	53.09	55.35	58.97	64.05	70.55	78.11	86.28	109.16	140.57	167.52	188.82	206.16	221.03	234.21
8th	56.26	58.67	62.51	67.96	74.89	82.98	91.72	116.28	150.12	178.45	200.08	217.68	232.80	246.27
9th	58.36	60.86	64.87	70.56	77.79	86.21	95.31	120.99	156.56	185.62	207.35	225.15	240.45	254.07
10th	59.40	62.00	66.02	71.85	79.24	87.82	97.11	123.41	159.84	189.15	210.95	228.80	244.21	257.92

Table 4. Temperature dependent IR-Drop (mV) of MLGNR and Cu interconnect for 16 nm technology and 50 µm length (global length).

Temperature (K) →	150	200	250	300	350	400	450	150	200	250	300	350	400	450
No of Stages ↓	Maximum Peak IR-Drop of MLGNR							Maximum Peak IR-Drop of Cu						
1st	34.38	35.59	37.45	40.05	43.30	46.93	50.81	61.60	75.60	87.74	98.66	108.77	118.06	126.79
2nd	64.59	66.85	70.42	75.31	81.41	88.20	95.54	115.58	141.31	163.38	183.20	201.39	218.29	234.07
3rd	91.33	94.64	99.65	106.70	115.41	125.18	135.65	164.42	201.07	232.16	258.20	280.07	298.95	315.48
4th	114.9	119.1	125.5	134.49	145.67	158.28	171.77	208.71	254.33	287.89	314.12	335.66	353.96	369.79
5th	135.4	140.3	148.1	158.91	172.36	187.45	203.77	248.10	295.87	328.67	353.73	374.09	391.27	406.10
6th	152.7	158.4	167.3	179.70	195.12	212.65	231.32	279.77	326.67	357.97	381.54	400.58	416.64	430.55
7th	166.7	173.1	182.9	196.73	213.86	233.40	254.31	303.48	348.89	378.61	400.79	418.68	433.80	446.96
8th	177.5	184.2	194.8	209.71	228.34	249.37	271.72	320.23	364.22	392.61	413.67	430.66	445.09	457.70
9th	184.6	191.9	203.0	218.59	238.06	260.20	283.05	330.91	373.84	401.28	421.58	437.97	451.93	464.19
10th	188.3	195.7	207.0	223.00	243.08	265.75	288.63	336.11	378.48	405.43	425.34	441.43	455.17	467.25
No of Stages	Minimum Peak IR-Drop of MLGNR							Minimum Peak IR-Drop of Cu						
1st	7.54	7.88	8.42	9.18	10.16	11.30	12.51	15.99	20.49	24.26	27.48	30.31	32.95	35.32
2nd	14.35	14.99	16.0	17.49	19.37	21.52	23.94	30.75	39.75	47.40	54.12	60.18	65.74	70.90
3rd	20.39	21.31	22.8	24.91	27.60	30.76	34.23	44.26	57.71	69.44	79.94	89.68	98.75	107.30
4th	25.71	26.92	28.8	31.42	34.92	38.91	43.40	56.47	74.28	90.26	104.90	118.61	131.65	144.19
5th	30.32	31.73	33.9	37.12	41.19	46.06	51.43	67.28	89.39	109.51	128.42	146.31	163.65	180.43
6th	34.16	35.73	38.2	41.88	46.55	52.01	58.23	76.55	102.66	126.85	149.76	171.80	193.21	214.11
7th	37.23	38.93	41.7	45.68	50.87	56.93	63.74	84.27	113.78	141.50	168.02	193.71	218.74	243.18
8th	39.53	41.38	44.4	48.53	54.11	60.65	68.00	90.13	122.39	153.04	182.47	211.03	238.86	266.08
9th	41.06	43.03	46.1	50.50	56.28	63.12	70.85	94.18	128.38	160.99	192.37	222.98	252.78	281.88
10th	41.83	43.85	47.0	51.49	57.36	64.36	72.27	96.21	131.37	165.02	197.50	229.03	259.87	289.99
No of Stages	Average IR-Drop of MLGNR							Average IR-Drop of Cu						
1st	20.96	21.73	22.93	24.61	26.73	29.11	31.66	38.79	48.04	56.00	63.07	69.54	75.50	81.05
2nd	39.47	40.92	43.21	46.40	50.39	54.86	59.74	73.16	90.53	105.39	118.66	130.78	142.01	152.48
3rd	55.86	57.97	61.23	65.80	71.50	77.97	84.94	104.34	129.39	150.80	169.07	184.87	198.85	211.39
4th	70.30	73.01	77.14	82.95	90.29	98.59	107.58	132.59	164.30	189.07	209.51	227.13	242.80	256.99
5th	82.86	86.01	91.00	98.01	106.77	116.75	127.60	157.69	192.63	219.09	241.07	260.20	277.46	293.26
6th	93.43	97.06	102.7	110.79	120.83	132.33	144.77	178.16	214.66	242.41	265.65	286.19	304.92	322.33
7th	101.96	106.01	112.3	121.20	132.36	145.16	159.02	193.87	231.33	260.05	284.40	306.19	326.27	345.07
8th	108.51	112.79	119.5	129.12	141.22	155.01	169.86	205.18	243.30	272.82	298.07	320.84	341.97	361.89
9th	112.83	117.46	124.5	134.54	147.17	161.66	176.95	212.54	251.11	281.13	306.97	330.47	352.35	373.03
10th	115.06	119.77	127.0	137.24	150.22	165.05	180.45	216.16	254.92	285.22	311.42	335.23	357.52	378.62

Table 5. Temperature dependent delay In MLGNR and Cu interconnects at different interconnects length Using 16 nm Technology. Delay Values Are In Ps.

Temperature (K) →	150	200	250	300	350	400	450	150	200	250	300	350	400	450
No of Stages ↓	MLGNR interconnect delay(5 µm-Local length)							Cu interconnect delay(5 µm-Local length)						
1st	3.74	3.75	3.76	3.77	3.78	3.79	3.82	3.86	3.94	4.03	4.12	4.20	4.28	4.37

2nd	6.05	6.06	6.09	6.11	6.16	6.21	6.27	6.41	6.68	6.94	7.21	7.47	7.73	8.00
3rd	8.01	8.08	8.09	8.18	8.32	8.42	8.58	8.95	9.65	10.30	10.87	11.48	12.03	12.60
4th	9.82	9.89	10.04	10.23	10.44	10.72	11.02	11.72	13.15	14.55	15.65	16.70	17.60	18.45
5th	12.48	12.64	12.80	13.11	13.50	13.95	14.50	15.80	17.80	19.65	21.10	22.40	23.50	24.65
6th	16.25	16.45	16.70	17.10	17.65	18.30	18.95	20.35	22.65	24.90	26.70	28.15	29.85	31.15
7th	19.95	20.15	20.50	21.05	21.75	22.55	23.25	25.05	27.70	30.30	32.70	34.20	36.05	37.80
8th	24.00	24.30	24.75	25.40	26.15	26.70	27.65	29.65	32.95	36.15	38.70	40.60	42.95	45.40
9th	27.75	28.10	28.60	29.25	30.30	31.15	32.30	34.45	38.40	42.30	45.15	47.70	50.50	54.05
10th	31.70	32.10	32.65	33.35	34.60	35.65	37.00	39.35	44.00	48.70	52.25	56.30	59.90	62.65
No of Stages	MLGNR interconnect delay(20 μm-Intermediate length)							Cu interconnect delay(20 μm-Intermediate length)						
1st	3.96	3.97	3.99	4.03	4.08	4.14	4.21	4.41	4.72	5.03	5.32	5.60	5.90	6.20
2nd	6.70	6.75	6.83	6.94	7.09	7.27	7.49	8.13	9.13	10.15	11.09	12.20	12.80	13.70
3rd	9.72	9.86	10.04	10.30	10.60	11.05	11.50	12.90	14.95	16.50	17.95	19.40	20.90	22.40
4th	13.25	13.50	13.95	14.55	15.20	15.95	16.75	18.85	21.75	24.15	26.70	28.40	30.50	32.50
5th	18.00	18.35	18.85	19.65	20.50	21.40	22.50	25.65	29.30	32.20	35.75	38.20	41.10	44.00
6th	22.90	23.30	24.00	24.90	26.00	27.10	28.25	32.15	36.90	40.75	45.00	47.60	51.30	56.60
7th	27.90	28.30	29.00	30.20	31.80	33.05	34.30	38.90	45.15	49.60	55.95	60.90	65.20	69.20
8th	33.20	33.65	34.50	36.10	37.90	39.15	40.80	46.50	54.45	62.00	66.80	72.30	79.60	86.10
9th	38.65	39.15	40.25	42.25	44.25	45.65	47.90	55.60	64.60	73.10	82.45	90.10	98.10	106.00
10th	44.30	44.95	46.30	48.70	50.80	53.20	56.60	64.35	78.55	88.95	99.15	108.00	118.00	128.00
No of Stages	MLGNR interconnect delay(50 μm-Global length)							Cu interconnect delay(50 μm-Global length)						
1st	4.34	4.38	4.43	4.52	4.64	4.77	4.93	5.40	6.10	6.80	7.51	8.20	8.80	9.20
2nd	7.92	8.040	8.23	8.49	8.84	9.26	9.77	11.40	13.40	15.00	16.21	17.40	18.50	19.60
3rd	12.45	12.70	13.05	13.64	14.40	15.20	16.05	18.30	22.10	25.40	27.69	29.70	31.80	34.50
4th	18.20	18.55	19.10	19.87	20.90	22.15	23.60	27.20	32.00	36.90	39.84	42.90	46.90	50.30
5th	24.35	24.90	26.00	26.68	27.85	29.95	31.85	36.40	43.40	48.80	53.52	61.00	67.80	72.60
6th	30.75	31.40	32.65	33.66	34.80	37.90	40.10	45.70	55.20	65.30	70.41	77.20	87.20	96.00
7th	37.30	38.20	39.50	41.15	42.85	46.10	48.90	57.50	68.20	79.50	90.76	100.10	111.00	121.50
8th	44.65	45.85	47.25	49.07	51.35	56.25	60.00	68.20	85.70	99.60	113.05	122.00	136.00	150.50
9th	53.05	54.60	56.90	59.10	62.50	66.05	70.60	84.40	104.00	121.00	136.61	151.00	168.50	184.50
10th	62.10	63.50	65.40	69.76	73.60	79.90	85.55	102.00	126.50	150.00	169.75	188.00	211.00	233.00

5. Conclusions

In this work, we have proposed a temperature dependent resistive model of MLGNR and Cu interconnect and analyzed the effect of temperature on power supply voltage drop (IR-drop). It is observed that with the increase in temperature, the resistance is increased for both MLGNR and Cu, but MLGNR shows significantly less increase than the Cu interconnects (~2–5× times lesser), which exhibits less power supply voltage variation and hence less impact on the timing of the circuits. It also reduces the power dissipation of MLGNR based power interconnects as compared with Cu.

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Conflict of Interest

The authors declare that there is no conflict of interest regarding the publication of this manuscript.

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