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Research article

Towards low-voltage organic thin film transistors (OTFTs) with solution-processed high-*k* dielectric and interface engineering

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Abstract: Although impressive progress has been made in improving the performance of organic thin film transistors (OTFTs), the high operation voltage resulting from the low gate capacitance density of traditional SiO_2 remains a severe limitation that hinders OTFTs' development in practical applications. In this regard, developing new materials with high-*k* characteristics at low cost is of great scientific and technological importance in the area of both academia and industry. Here, we introduce a simple solution-based technique to fabricate high-*k* metal oxide dielectric system (ATO) at low-temperature, which can be used effectively to realize low-voltage operation of OTFTs. On the other hand, it is well known that the properties of the dielectric/semiconductor and electrode/semiconductor interfaces are crucial in controlling the electrical properties of OTFTs. By optimizing the above two interfaces with octadecylphosphonic acid (ODPA) self-assembled monolayer (SAM) and properly modified low-cost Cu, obviously improved device performance is attained in our low-voltage OTFTs. Further more, organic electronic devices on flexible substrates have attracted much attention due to their low-cost, rollability, large-area processability, and so on. Basing on the above results, outstanding electrical performance is achieved in flexible devices. Our studies demonstrate an effective way to realize low-voltage, high-performance OTFTs at low-cost.

Keywords: high-*k*; solution processed; low voltage; OTFTs; interface engineering; flexible

1. Introduction

During the past decades, rapid progress has been achieved in both the designing of novel organic semiconducting materials and the optimization of device fabrication techniques for organic thin film transistors (OTFTs) due to their potential applications in low-cost and flexible consumable electronics, such as such as RFID tags, flat panel displayers, and portable electronics [1–4]. However, the high operation voltage resulting from intrinsically low charge carrier mobility of organic semiconductors and the small gate capacitance density of traditional SiO2 remains a severe limitation that hinders their development in the market of commercial electronics [5]. This issue can be addressed through increasing the capacitance density of the gate dielectrics (C_i) by means of either increasing the dielectric constant (k) or decreasing the thickness (d) ($C_i = \varepsilon_0 k/d$). Practically, using high-k dielectrics instead of ultra-thin dielectrics is a promising choice, and much research interest has been devoted into this area. Metal oxides are important members of high-k dielectrics. Traditional fabrication routes for high-k metal-oxide dielectrics, such as atomic layer deposition [6], radio-frequency magnetron sputtering [7] and chemical vapor deposition [8], require expensive, high-vacuum equipment, and are time consuming to produce functioning layers. Therefore, it is of significant importance to develop a low-temperature, solution-based technique for the fabrication of high-k metal-oxides as gate dielectrics, in order to turn OTFTs into more reliable applications for low-cost, large-area devices.

Besides the development in synthesizing high-performance organic semiconductors and the gate dielectrics, much effort has been devoted to improve the device performance by optimizing the device performance through interface engineering [9–12]. Basically, two interfaces, i.e. organic semiconductor/dielectric interface and source-drain (S/D) electrode/organic semiconductor interface, are involved in the processes of charge transportation and injection/extraction. The native high-k metal oxide dielectric surface usually contains hydroxyl groups (OH^-), which act as defect sites, trapping charge carriers in the channel or inducing undesired charge carriers into the channel [13,14,15]. This issue can be overcome by introducing a self-assembled monolayer (SAM) at the interface between dielectrics and organic semiconductors, which can simultaneously passivate the defects and modify the oxide surface, resulting in enhanced device performance [16,17,18]. Among diverse SAMs, phosphonic acid headed alkylate has shown great advantages of readily chemisorbed onto metal-oxide surface [19,20,21] high thermal stability (~ 400 ^oC) [22], and other unique merits including better stability to moisture, less tendency of self-aggregation and unlimited by the densed surface hydroxyl groups [23].For the interface between S/D electrode/semicondcutor, one should be aware of two different circumstances. For efficient hole injectoin, an electrode material with enough high work function (W_F) that can be aligned with the highest occupied molecular obital (HOMO) of organic semiconductor is preferred. On the other hand, for efficient electron injection, the W_F of the electrode material should be low enough to align with the lowest unoccupied molecular orbital (LUMO) of organic materials. Moreover, to synchronize with the already established Si based microelectronic industry, it would be easier to realize large scale production of organic electronic devices if Cu can be used as the S/D electrodes of OTFTs. However, Cu is generally believed to be unsuitable as the S/D electrodes material due to its low work function (4.2 eV) [24],which results in large injection barrier when contacting with most p-type and n-type organic semiconductors, thus deteriorating device performance. To address this dilema, chemical modifications at the interface of Cu and orgnaic semiconductor have attracted much attention in

order to improve the device performance [25,26].

In addition, the inherent mechanical flexibility and low-temperature processibility of organic semiconductors stimulate the attempts of integration of OTFTs with bendable substrates, which is of great technical significance because they are fundamental building blocks of most practical electronic devices. Furthermore, to realize printability in future organic electronics industry, it is necessary to develop low-temperature, solution-processible dielectric materials that can be compatible with the high-throughput production, such as roll-to-roll processing.

In this paper, we will give a brief review of our recent research results on solution-processed high-*k* metal-oxide dielectric and the related low-voltage OTFTs. At first, a sol-gel based high-*k* metal-oxide dielectric will be introduced, which can then be used effectively to realize low-voltage operation of OTFTs [27,28,29]. Secondly, highly improved device performance using low-cost Cu as S/D electrodes for both p- and n-type organic semiconductors is demonstrated through interface engineering [30,31]. Finally, based on the above findings, flexible pentacene OTFTs on polyimide (PI) substrates are successfully fabricated with excellent device performance [32]. Our results demonstrate a simple and feasible route to fabricate high-performance OTFTs with solution-processed dielectric and low-cost electrode material, which is of great technical importance to realize large-scale application of organic electronics.

2. Materials and Method

All the chemicals used in this paper are bought from Aldrich without further clarification. Titanium oxide (TiO_x) sol was prepared by dissolving titanium (IV) isopropoxide (TIP) ($Ti(OC_3H_7)_4$, 99.99%) into a mixture of methanol and acetic acid in a concentration of about 0.1 mol/L, and then vigorously stirred for 24 h in ambient conditions. Aluminum oxide (Al_2O_y) sol was prepared by dissolving aluminum nitrate nonahydrate ($Al(NO_3)_3$•$9H_2O$, 99.99%) into 2-methoxylethanol in a concentration of about 0.5 mol/L and then stirred for 12 h in ambient conditions. The TiO_x layer was deposited by spin-coating the TiO_x sol onto the cleaned n^{++}-Si substrates at 5000 r/min for 40 s, followed by baking at 200 ± 5 ℃ for 5 min to ensure the hydrolyzation and decomposition of the precursor. Subsequently, the Al_2O_y layer was deposited by spin-coating the Al_2O_y sol onto the cooled TiO_x-coated substrates and then baked at the same condition as that of TiO_x. The obtained double layer Al_2O_y/TiO_x is referred to ATO for short hereafter. For ATO deposited on flexible PI substrates, the spin-coating condition is the same as that on n^{++}-Si substrates. Prior to ATO deposition, 5 nm Cr and 20 nm Au was vacuum deposited successively on PI substrates under a vacuum of 3×10^{-4} Pa. For SAM modification, the as prepared ATO substrates were immediately immersed in an octadecylphosphonic acid (ODPA) solution (5 mmol/L in isopropanol) for 20 h, followed by a 48 h curing at 145 ℃ in vacuum, and then washed by isopropanol ultrasonically for 6 min and blown dry by N_2 gas for use.

Bottom-gate top-contact (BGTC) OTFTs were fabricated by thermally deposition of 30 nm organic semiconductors onto the substrates with temperatures of 180 ℃ for copper phthalocyanine (CuPc), 60 ℃ for pentacene and and 110 ℃ for C60, respectively, followed by deposition of S/D electrodes through shadow mask. For pentacene TFTs, the *in-situ* modified Cu electrodes (*M*-Cu) was formed by firstly deposited onto the pentacene layer under a gradient deposition pressure from 5×10^{-3} Pa to about 3×10^{-4} Pa, and then 10 nm Au was deposited onto the above *M*-Cu without breaking the chamber vacuum. For C_{60} TFTs, a branched polyethylenimine (PEI, M_W =

25000)/methanol solution was spin-coated onto the C60 film before Cu electrodes deposition.

The electrical characteristics of the C_{60} OTFTs were measured by Keithley 4200 SCS. The frequency-dependent capacitance of the dielectrics was measured by HP 4284A in a frequency range of 20 Hz-100k Hz. The morphologies of the thin films were characterized by atomic force microscopy (AFM, Nanoscope IIIa) in tapping mode. The surface potential was recorded by KPFM method using Pt coated tips. The X-ray diffraction (XRD) patterns were obtained on an X-ray diffractometer (Simens, D5000) using Cu *Kα* radiation (λ = 0.154 nm) at a scan rate of 0.02^o 2θ/s. The two-dimensional grazing incidence X-ray diffraction (GIXD) pattern was obtained at beamline BL14B1 (λ = 1.24 Å) of the Shanghai Synchrotron Radiation Facility with an incident angle of 0.15^o.

3. Results and Discussion

Figure 1a shows the tapping mode AFM image of the ATO. As seen, the ATO exhibits a homogenous and smooth surface with a root mean square (RMS) roughness value of ~ 0.22 nm in an area of 5 μm × 5 μm, as smooth as that of the n^{++}-Si substrate with 300 nm SiO_2 (RMS ~ 0.19 nm), and no obvious surface defects and pinholes are observed. Figure 1b shows the atomic composition profiles of O, Al, C, Ti, and Si as a function of etching time obtained from the bilayer Al_2O_y/TiO_x. As seen, the atomic ratio of Al to O in region I is about 2:2.7, giving an y value of 2.7. With increasing etching time, the intermixing layer containing Al_2O_y and TiO_x, which can be observed in region II. Beneath region II, a more complex intermediate layer containing Al, Ti, Si, and O, marked as region III, is observed. The total thickness of the bilayer Al_2O_y/TiO_x is estimated to be 45 nm (measured by AFM). The inset of Figure 1b shows the depth profiles of atomic composition obtained from a 12 nm thick, single layer TiO_x. In the case of single layer TiO_x, the atomic ratio of Ti and Si to O is smaller than 2, suggesting that some oxygen vacancies exist in the transition layer.

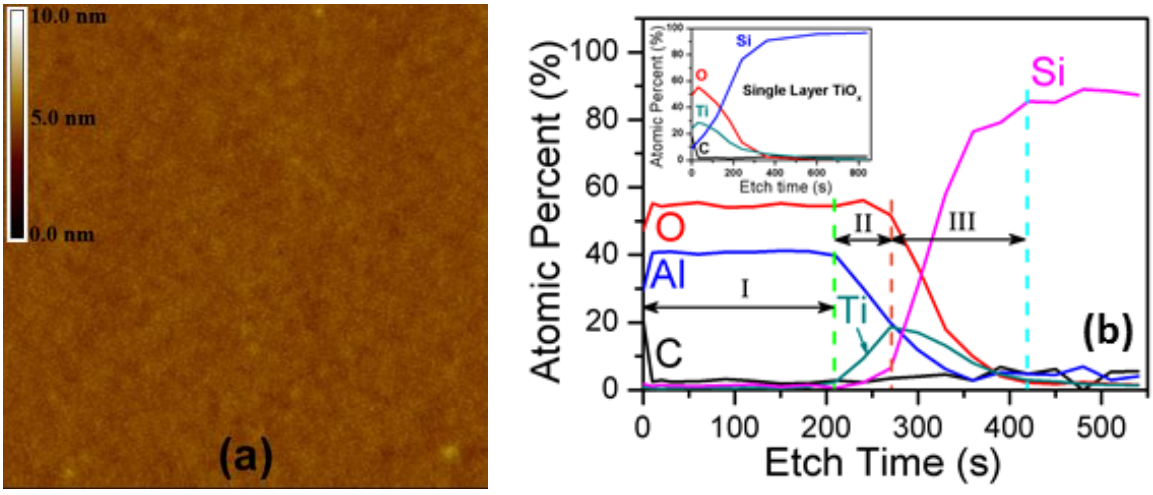

Figure 1. (a) AFM image and (b) XPS depth profile of ATO; the inset of (b) shows the XPS depth profile of single layer TiO_x.

To characterize the electrical properties of the solution-processed dielectric, we fabricate an Au/ATO/n^{++}-Si (MIM) sandwiched structure and test its current-voltage and capacitance-frequency

characteristics. Figure 2a shows the typical leakage current density versus bias voltage plots of a single layer TiO_x and ATO. The asymmetrical leakage of single layer TiO_x is likely due to the zero conduction band offset at the Si/TiO_x interface [8] and the different work function of Si and Au, as can be seen from Figure 2a. After deposition of the Al_2O_y layer, the leakage current was reduced by 4 orders of magnitude under positive bias of +2 V. The reduction of leakage is due to the blocking of electron conduction path by the Al_2O_y layer. In addition, two distinct regions can be observed in both single layer and bilayer dielectrics, as noted with A and B. Similar phenomena have been extensively studied by Mahapatra et al, and according to their theory, the conduction in region A is governed by a charge hopping process and the conduction in region B is dominated by both Proole-Frenkel emission and trap assisted tunneling processes [18]. Figure 2b exhibits the frequency dependence of capacitance density for the MIM structure under different bias voltages. For single layer TiO_x, under a bias voltage of 0 V, the total capacitance density is ~ 850 nF/cm^2 at 20 Hz, and an equivalent *k* value of about 12 can be obtained. As for the bilayer Al_2O_y/TiO_x, capacitance density is reduced owing to the introduction of another capacitor (i.e. Al_2O_y) in series. In addition, the observed voltage dependence capacitance density can be attributed to the variation of space charge distribution, i.e., the redistribution of oxygen vacancies in the film driven by the applied voltages [19]. This positively charged oxygen vacancy accumulation layer induces additional electrons at the bottom electrode, forming an "electric double-layer" (EDL) capacitor. For better understanding the voltage and frequency dependent capacitance density, a simple model with equivalent circuit is proposed in the inset of Figure 2b. Under an AC bias with sufficiently low frequencies, the oxygen vacancies will have enough time to respond to the bias change and go back and forth in the vicinity of the space charge layer, which can be viewed as a macroscopic dipole oscillating with the field. The lower the frequency is, the larger the distance of oscillation is, and ultimately giving rise to larger the capacitance density.

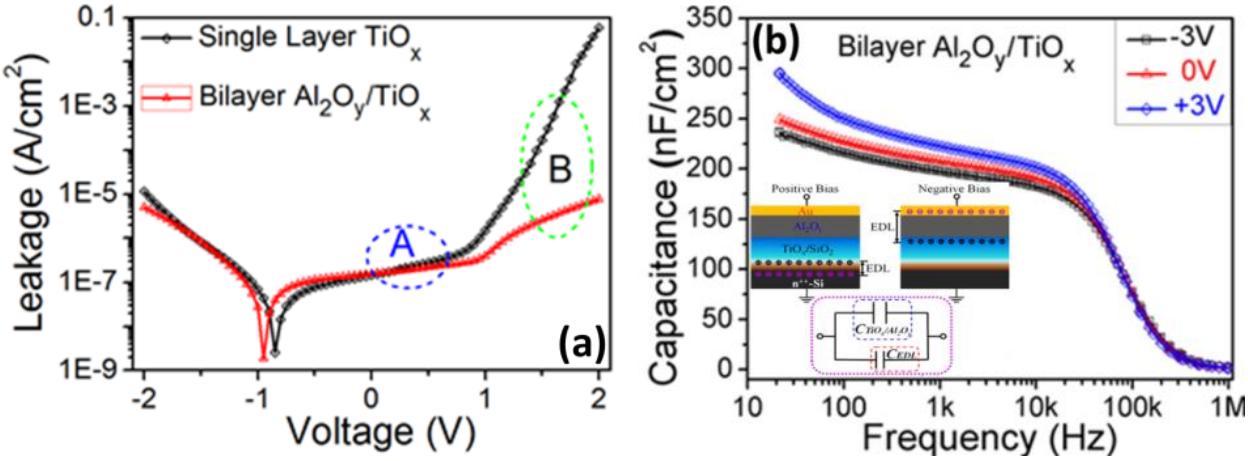

Figure 2. (a) Leakage current density and (b) frequency dependent capacitance density characteristics of ATO; the inset of (b) is the proposed EDL model and equivalent circuit.

To demonstrate the effectiveness of our solution-processed ATO dielectric, bottom-gate, top-contact (BGTC) CuPc OTFTs with Au S/D electrodes are fabricated. The upper two figures of Figure 3a show the output and transfer curves of a representative CuPc OTFT. Due to the high

capacitance of ATO, the device can work effectively at operation voltages as low as −2 V. Clear linear and saturation regions can be observed from the output curves. From the transfer curve, the μ, V_T, on/off ratio, and *SS* are estimated to be 0.15 cm^2/Vs, −1.1 V, 5 × 10^3, and 232 mV/dec, respectively. Comparatively, the 300 nm SiO_2 based CuPc device is also fabricated, and the obtained μ, V_T, on/off ratio and *SS* are 2.8 × 10^{-3} cm^2/Vs, −6.0 V, 10^3 and 5.9 V/dec, respectively, under a high voltage of −40 V, as shown in the lower part of Figure 3a. Apparently, the device on ATO exhibits much higher performance than that on 300 nm SiO_2. The electronic property of OFETs can be influenced by several aspects, such as dielectric surface property, organic layer crystal structures, and

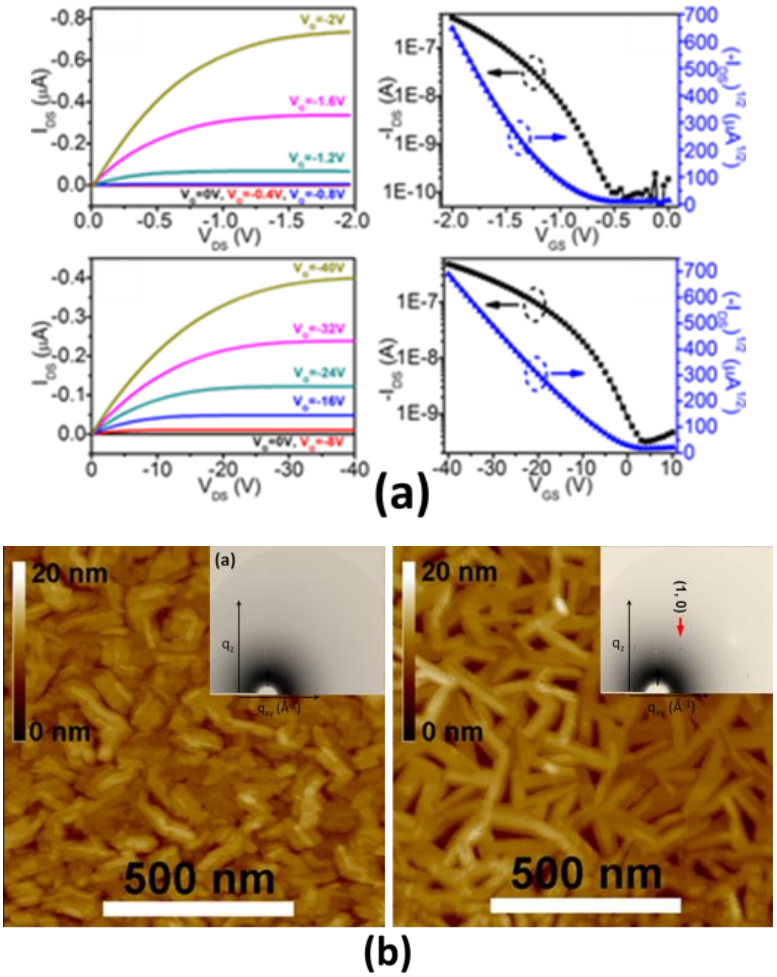

Figure 3. (a) Output and transfer curves of CuPc OTFTs on ATO (the upper two) and 300 nm SiO_2 (the lower two), (b) AFM image so 2.4 nm CuPc on ATO (left) and 300 nm SiO2 (right); the inset in (b) corresponds to their respective GIXD pattern.

semiconductor-dielectric interface characteristics. AFM and XRD studies reveal that the ATO and SiO2 have similar surface roughness, and the CuPc deposited on both dielectric give the same crystal structure. To get a deeper insight into the difference in device performance, the interface between CuPc and dielectrics are characterized, and the results are shown in Figure 3b. As seen, when deposited on SiO_2, the growth of CuPc molecules exhibits the Stranski-Krastanov mode [33], which occurs when the interaction between the molecules and the substrates are stronger than that between

the molecules [34]. On the other hand, when deposited on ATO, the growth of CuPc molecules can be described by the Volmer-Veber growth mode [33], in which the deposited molecules are more strongly bonding to each other than to the substrate [34]. In addition, the insets of Figure 3b show the GIXD patterns of 2.4 nm CuPc on both dielectrics. No diffraction peak is found in the CuPc on SiO_2, indicating that the amorphous in-plane structure for the first several monolayers. On the other hand, a clear diffraction peak noted as (1,0) can be observed from the pattern of the CuPc film on ATO (indicated by the red arrow), revealing a crystalline structure of the first several monolayers of CuPc. The ordered in-plane structure and the interconnected network of CuPc on ATO thus account for the highly enhanced device characteristics of our devices, because the charge transport at the conducting channel is mainly located at the first several monolayers at the interface [35,36].

We have introduced the low-temperature (~ 200 ^{o}C) solution-processed high-*k* ATO dielectric system, and the CuPc TFTs with this gate dielectric show good electrical performance under an operation voltage as low as −2 V. However, native oxide dielectric surface usually contains hydroxyl groups (OH^{-}), which act as defect sites, trapping charge carriers in the semiconductor/dielectric interface or inducing undesired charge carriers into the interface [13,14,15].To further improve the device performance, surface modification is employed to optimize the interface property. Here we use ODPA to modify the surface of ATO. Figure 4 shows the leakage and frequency dependent capacitance characteristics ODPA modified ATO (ODPA/ATO) and bare ATO. As shown in Figure 4a, after ODPA modification, the leakage current density can be significantly suppressed by more than one order of magnitude under a bias of 2 V. The decrease in leakage current density indicates the formation of densely packed ODPA molecules on the surface of alumina in ATO. The static contact angle of DI water on ODPA/ATO is about 110^{o}, while that on bare ATO is about 35^{o}, further confirming the formation of high quality SAM [37]. The C_i of ODPA/ATO is 200 nF/cm^2, while that of bare ATO is 250 nF/cm^2, as can be seen from Figure 4b. The low leakage, large contact angle (low surface energy), and high capacitance density of the ODPA/ATO system endows it with suitability for high-performance low-voltage OTFTs.

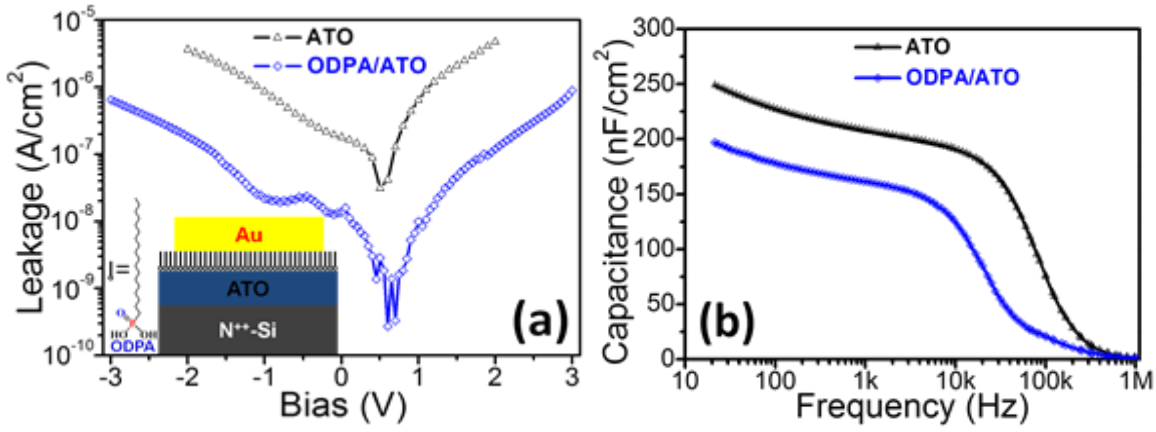

Figure 4. (a) leakage and (b) frequency dependent capacitance density of ATO and ODPA/ATO.

Besides the dielectric properties, the choices of S/D electrode materials are also crucial in achieving high-performance devices. Generally speaking, for p-type organic semiconductors, the electrodes need to have high enough WF to align with the HOMO of the semiconductor. Au is the

most widely used S/D electrode material for pentacene TFTs because of its inherently high work function, good conductivity and environmental stability. However, the high cost of Au hinders its use in realistic applications. Furthermore, during thermal deposition, the severe diffusion of Au into pentacene film results in high resistive grain boundaries and forms interface dipoles by doping the upper layer pentacene, and thus deteriorating the device perofrmance [38–41]. These unfavorable issues can be overcome by using *in-situ* modified low-cost Cu (*M*-Cu) as S/D electrodes, in which the Cu atoms are *in-situ* oxidized by residual oxygen species in the chamber at low vacuum atmosphere. The CuO_x formed in the interface of Cu and pentacene is believed to function as a modification layer owing to its high valence band. To verify the validity of *M*-Cu S/D electrodes, the pentacene TFTs are fabircated the their electrical performance is shown in Figure 5a. Owing to the high capacitance density of the ODPA/ATO (200 nF/cm^2), the devices worked very well under a low gate voltage of −3 V. For the device with *M*-Cu electrodes, the μ and V_T are estimated to be 1.0 cm^2/Vs, 156 mV/dec and −0.62 V, respectively. In comparison, for the device with Au electrodes, the μ and V_T are determined to be 0.71 cm^2/Vs and −1.4 V, respectively. As clearly seen, the device with *M*-Cu electrodes exhibits much higher performance as compared to that with Au electrodes. Because both devices were fabricated under the same condition, excepting the S/D electrodes, it is plausibly to ascribe the above observations to the interaction between electrode and organic semiconductor. To clarify the relationship between electronic performance of devices and S/D electrodes, we estimate the contact resistance (R_C) with the transfer line method (TLM) in the linear region [42]. Figure 5b shows the dependence of total resistance on channel length of devices with different electrodes, and R_C is obtained from the intercept by extrapolating the resistance line to the zero channel length. For Au electrodes, the R_C is estimated to be about 0.41 MΩ. For *M*-Cu electrodes, on the other hand, the R_C is drastically reduced, estimated to be about 0.11 MΩ. During thermal deposition, hot Au atoms usually diffuse into the pentacene film, thus resulting in high resistive grain boundaries and forming interface dipoles by doping the upper layer pentacene [41,43,44]. However, when using *M*-Cu as S/D electrodes, Cu atoms are oxidized by residual oxygen species in the chamber due to the low vacuum atmosphere. As a result, a thin layer of CuO_x is *in-situ* formed at the initial stage of thermal deposition instead of pure Cu. XPS results revealed that the interface CuOx is mainly composed of Cu_2O. Cu_2O is a widely studied p-type semiconductor with valence band (*VB*) position locating around 5.4 eV [45], which is well aligned with the highest occupied molecular orbital (HOMO) of pentacene (5.0 eV) [46]. Consequently, the *in-situ* oxidized CuO_x layer in *M*-Cu electrodes can act as an effective hole-injection layer, resulting in optimized electrode/pentacene contact, and hence improving the device performance. To better understand the mechanism, the band diagram of different electrode materials are given in Figure 5c. For Au electrodes (left part), an typical value of interface dipole (Δ) of 0.5 eV is adopted [41]. Due to the physical and chemical damage caused in the interface of Au/pentacene, some deep trap sites are induced. When *M*-Cu is used as the S/D electrodes (right part), the thin layer of Cu_2O in the interface serves as a effective hole-injection layer.

High-performance p-channel pentacene OTFTs have been demonstrated with low-cost Cu S/D electrodes through interface engineering. However, from the point of view of integrated circuits design basing on the industrial complementary metal oxide semiconductor (CMOS) technique, both p-channel and n-channel OTFTs are desired. For efficient electron injection into n-type organic semiconductors, the work function (W_F) of the electrode should be low enough to align with the lowest unoccupied molecular orbital (LUMO) of organic materials, thus lowering the electron

injection barrier and forming the Ohmic contact. Zhou et al. reported that the W_F of conductors, such as Au, Ag and ITO, can be substantially reduced upon simply spin-coating a thin layer of polyethylenimine ethoxylated (PEIE) or branched polyethylenimine (PEI), which containing aliphatic amine groups, and obviously improved device performance was observed by using the modified conductors as electrodes owing to the enhanced electron injection at the electrode/semiconductor interface [47]. Here, as inspired by the same idea, we employ PEI to modify Cu to see whether it can be used as an effective S/D electrodes for n-type organic semiconductors.To evaluate the effect of PEI modification on the surface performance of Cu, KPFM was used to record the W_F variation by measuring the contact potential difference (CPD) between the sample and the reference Au film. Before measurements, the W_F of Au is calibrated by freshly peeled highly ordered pyrolytic graphite (HOPG) with a known W_F of 4.6 eV [48]. The calibration reveals that the W_F of Au is determined to be 4.7 eV, which is in good agreement with those reported values due to existence of surface contaminates when exposing to ambient atmosphere [49,50]. Figure 6 gives the comparison of KPFM images of Cu before and after PEI modification. As seen in Figure 6a, the surface potential of thermally deposited Cu is about 50 mV higher than that of Au, indicating that the W_F of Cu is 4.65 eV, which is consistent with the reported values [51,52]. Surprisingly, after PEI

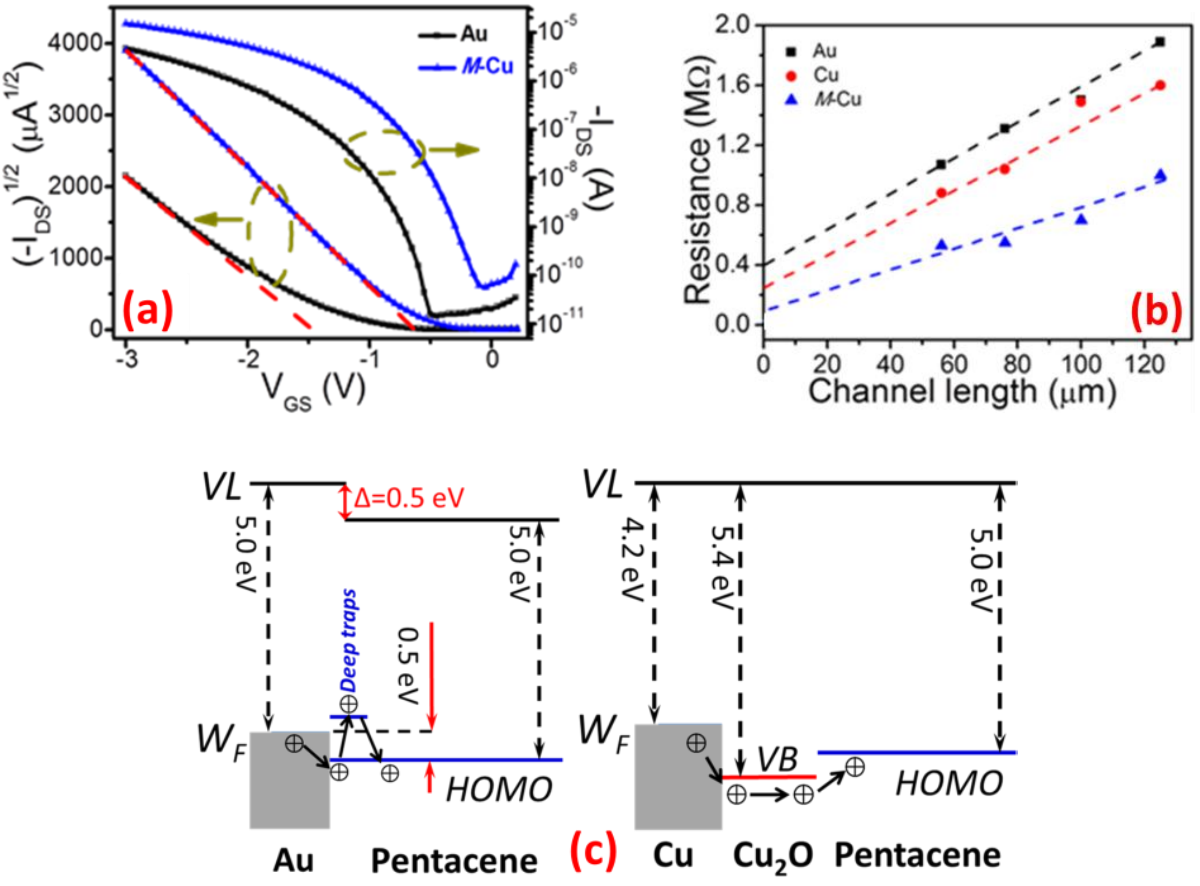

Figure 5. (a) Transfer curves of pentacene OTFTs with Au and *M*-Cu S/D electrodes, (b) transfer line method (TLM) polts of pentancene TFTs with different S/D electrodes and (c) schematic energy diagrams of Au/pentacne (left) and *M*-Cu/pentacene (right).

modification, the CPD between Au and the modified Cu increases to about 420 mV, denoting a drastic decrease in W_F of Cu to 4.28 eV, as shown in Figure 6b. It is known that the amine group has a strong electron donating feature, and there will be a charge-transfer interaction between amine group and the Cu surface, thus resulting in a reduced W_F [47,53]. On the other hand, the intrinsic molecular dipole within the polymer may also contribute to the decreased W_F of Cu [54,55].

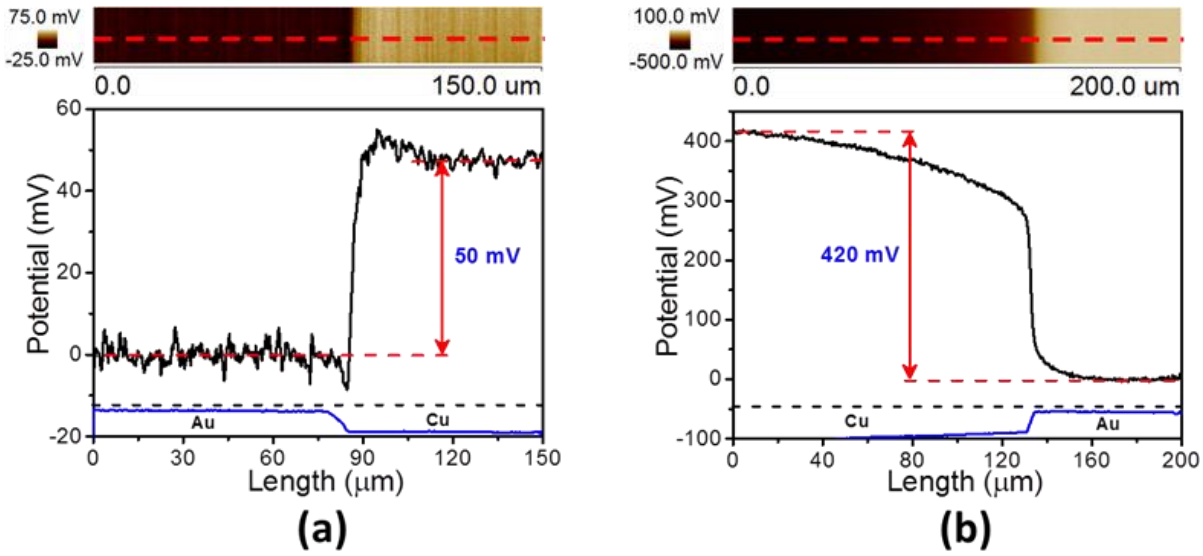

Figure 6. KPFM results of Cu before (a) and after PEI modification (b); the lower parts give the topography of each device.

Figure 7 gives the transfer characteristics of top-contact C_{60} based OTFTs fabricated on the ODPA/ATO using Cu and PEI modified Cu as S/D electrodes. As seen, all devices can work perfectly under a gate voltage (V_{GS}) as low as 3 V due to the high capacitance density of the gate dielectric. When Cu is used as S/D electrodes, the electron mobility (μ_e) is determined to be 1.0 cm^2/Vs. Surprisingly, after modifying Cu with 0.1% (wt%) PEI solution, the μ_e increases to about 1.5 cm^2/Vs, indicating that PEI modification can effectively enhance the device performance. Noting that methanol is used as the solvent in our experiment, which might also impact the resultant device property. To find out the dominant influencing factor, a control sample with only methanol spin-coating on the surface of C_{60} before the deposition of Cu S/D electrodes is also fabricated for comparison. The electrical performance of the control sample, however, shows a slight degradation (with μ_e of 0.7 cm^2/Vs) against the above PEI modified one, which can be due to the residue of polar methanol molecules in the C_{60} film acting as the charge trapping centers for both holes and electrons [56]. The above results confirm that the improving in device performance is resulted from the PEI modification. Further studies reveal that the device performance also strongly depends on the concentration of PEI solution. As can be seen from Figure 7c, when 0.2% PEI solution is used, the μ_e increases to about 2.4 cm^2/Vs, which is obviously higher than that of the device with Cu S/D electrodes. With further increase the concentration of PEI solution, the μ_e reaches the peak value of about 3.2 cm^2/Vs at 0.4% and then followed by a decline to about 1.1 cm^2/Vs at 0.8%, as shown in Figure 7d and e. For better understanding, the relationship between electron mobility of C_{60} TFTs and the PEI concentration is plotted in Figure 7f. As seen, the mobility increases monotonously with

the concentration of PEI in the beginning, and then reaches the highest value at 0.4%. After that, a rapid depression is evidenced with further increasing the concentration to 0.8%. As far as we know, the obtained electron mobility value of 3.2 cm^2/Vs is the highest one achieved in C_{60} TFTs basing on ODPA modified dielectrics [57,58,59].

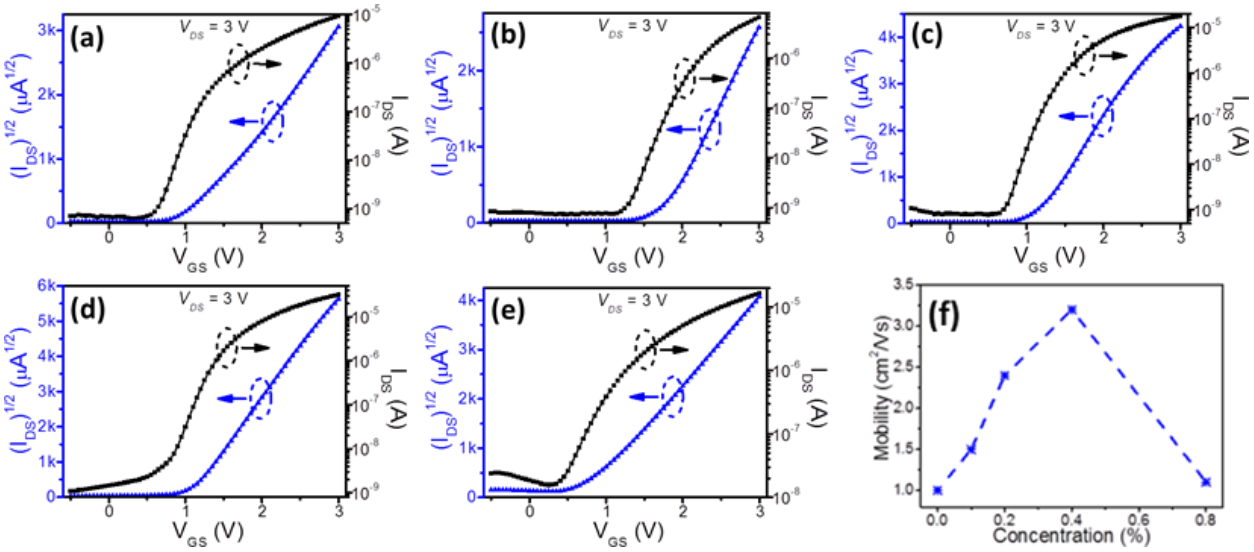

Figure 7. Transfer characteristics of C_{60} OTFTs using Cu (a) and PEI modified Cu with various concentrations as S/D electrodes, (b), (c), (d) and (e) correspond to concentrations of 0.1%, 0.2%, 0.4% and 0.8%, respectively; (f) plot of PEI concentration dependent mobility.

To further explore the relationship between PEI modification and the device performance, the relationship between R_C against PEI concentration are plotted in Figure 8a. As can be seen from Figure 8a, when Cu is used as S/D electrodes, the device shows a R_C of about 2.2 $\times 10^{-1}$ MΩ. After modified by the 0.1% PEI solution, the R_C decreases drastically to about 6.1 $\times 10^{-2}$ MΩ, which is much lower than that of the unmodified device. The decline in R_C after PEI modification can be attributed to the decreased W_F of Cu from 4.65 eV to 4.27 eV, which resulting in a lowered electron injection barrier at the interface of Cu/C_{60} and then an improved device performance. With further increasing the concentration of PEI, the R_C decreases monotonously, and a R_C of only 2.7 $\times 10^{-3}$ MΩ is obtained at 0.4%. Interestingly, the average linear region channel conductance of devices with 0 % to 0.4 % PEI is estimated to be 16.7 ± 1.1 μS, thus eliminating the doping effect of PEI to C_{60}. However, an increased *Rc* of 1.0 $\times 10^{-3}$ MΩ is observed with PEI concentration of 0.8%, which can be resulted from the resistive PEI layer. For clarity, the dependence of R_C on PEI concentration is plotted in the upper inset of Figure 8a. The variation of R_C with PEI concentration is consistent with the electrical characteristics of the corresponding device. In order to provide a clear picture on the mechanism of improvement in device performance, the band structures at the interfaces of Cu/C_{60} before and after 0.4% PEI modification are illustrated in Figure 8b. For C_{60}, a LUMO of 4.5 eV is adopted in our present study [60,61,62]. The left part of Figure 8b shows the band structure of Cu/C_{60} interface without modification, in which E_{Vac} and E_F denote the vacuum level and Fermi level, respectively.

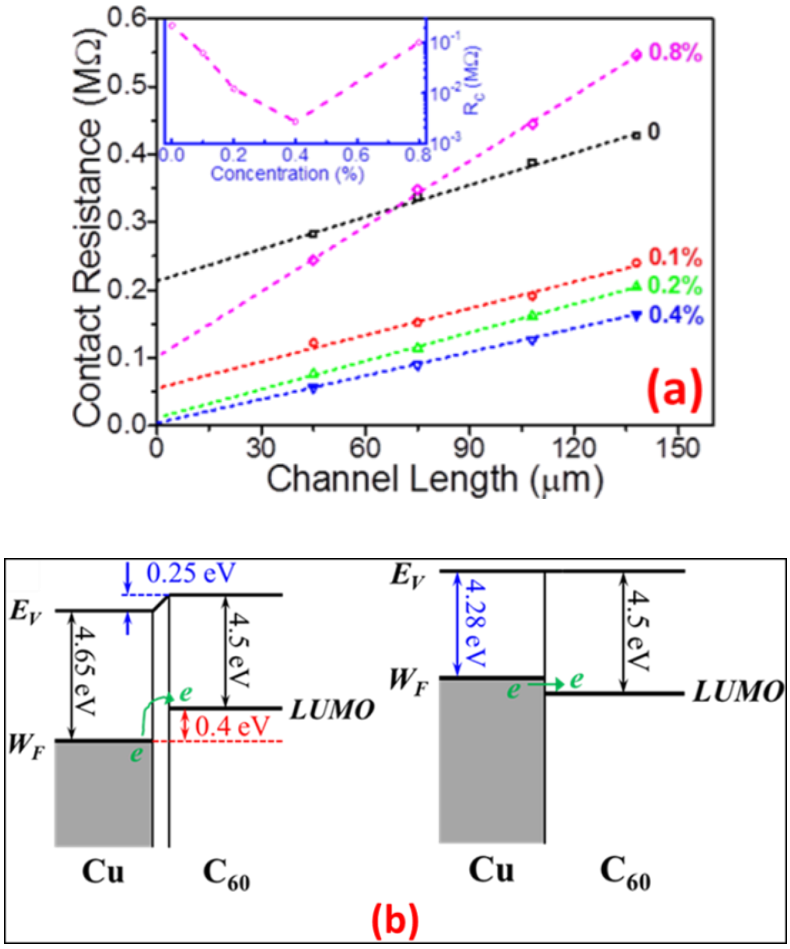

Figure 8. (a) Transfer line method (TLM) plots of C_{60} OTFTs modified by various PEI concentrations and (b) energy level diagrams at the interface of Cu/C_{60} before (left) and after (right) PEI modification; the inset of (a) shows the relationship between the contact resistance and PEI concentration.

As seen, an electron injection barrier of 0.40 eV is observed between Cu and C_{60} due to the existence of interface dipole [63], which is then responsible for the poor device performance and the high contact resistance. In contrast, as depicted in the right part of Figure 8b, after modified by PEI, an electron injection favorable band structure is achieved due to the combining effects of reduced W_F of Cu to 4.28 eV and suppression of interface dipoles. Consequently, obviously enhanced electrical properties as well as drastically decreased R_C can be expected with the resultant device.

The thermal stability of the above PEI modified device is also characterized and the results are given in Figure 9. To eliminate the influence of oxygen and water vapor in air, the device is encapsulated by a layer of 200 nm CYTOP. As seen, the elevated temperature seems to show no obvious influence on the turn-on voltage of the device. On the other hand, the off-current increases with temperature, which can be due to combined effects of increased conductance of C_{60} film and gate leakage at higher temperatures. The inset of Figure 9 plots the temperature dependent mobility of the device. Notably, after CYTOP encapsulation, the mobility decreases to about 1.0 cm^2/Vs, which is presumably due to the residue of CYTOP solvent in the C_{60} film. The mobility of device increases with the temperature initially until 100 ^oC, and then declines monotonously. Strikingly, at

temperature as high as 200 ^{o}C, our device can still work effectively without any degradation in mobility as compared to the original device, manifesting its outstanding thermal stability. The high thermal stability of the PEI modified device is of great importance to the application of OTFTs in biomedical equipment, in which a high temperature (120 ^{o}C) is needed to realize asepsis and prevent infection [64].

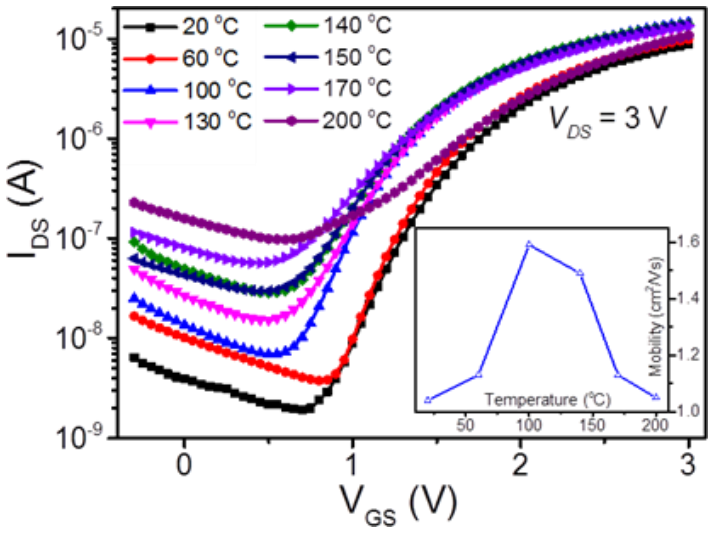

Figure 9. Variation of transfer curves of PEI modified devices with temperature; the inset shows the relationship between temperature and mobility.

Low-voltage, flexibility and low-cost are essential prerequisites for large scale application of organic thin film transistors (OTFTs) in future low-end electronics. Previously, we have demonstrated high-performance low-voltage OTFTs with ODPA/ATO dielectric and low-cost Cu S/D electrodes. In this part, we will show that, basing on these findings, high-performance flexible OTFTs can also be realized. The ATO dielectric on Au coated PI substrates was fabricated by spin coating TiO_x sol (5000 r/min, 40 s) and Al_2O_y sol (5000 r/min, 20 s) in sequence, and then baked at 200 ± 5 ℃ for 3 min, followed by ODPA modification. Figure 10 shows the leakage current density and the capacitance density characteristics of the ODPA/ATO on flexible substrates. As can be seen form Figure 10a, after ODPA modification, the leakage current density can be effectively suppressed by one order of magnitude under bias voltages of ±3V, indicating that the ODPA molecules assemble densely on the surface of alumina in ATO. The large DI H_2O contact angle (110 ^{o}C) of the ODPA/ATO also signifies its low surface energy, which is believed to be critical in enhancing the device properties [65]. Figure 10b shows the frequency dependent capacitance density of ODPA/ATO. A slight increase in capacitance density with decreasing frequency is observed in both ATO and ODPA/ATO, which can be due to the Maxwell-Wagner space charge polarization in the ATO layer [27,66,67]. The obtained C_i value is 180 nF/cm^2 for ODPA/ATO at 20 Hz, which is in good agreement with the calculated one by using the equation $1/C_{total}=1/C_{ATO}+1/C_{ODPA}$ [68]. Such a high capacitance density is sufficient to induce adequate charge carriers at a low voltage.

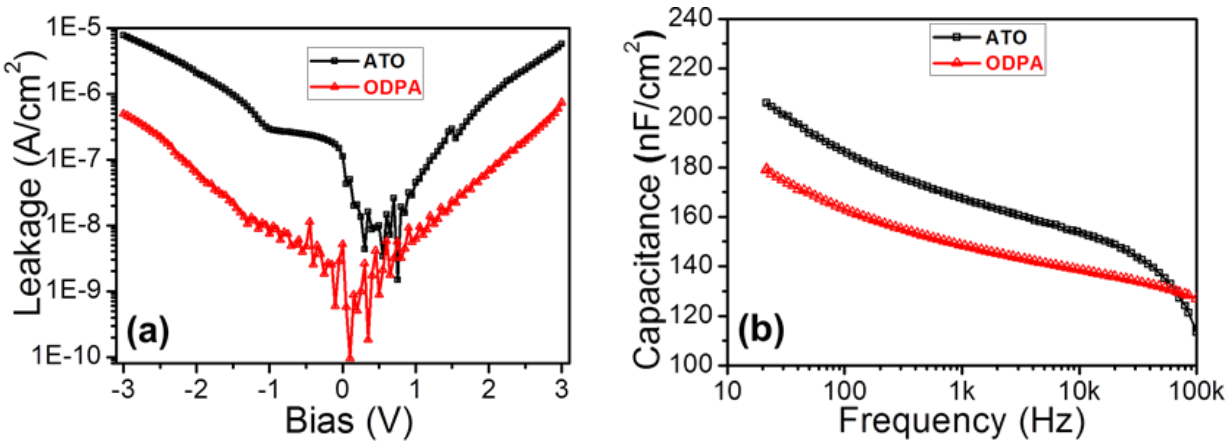

Figure 10. (a) Leakage and (b) frequency dependent capacitance density characteristics of ATO and ODPA/ATO.

Figure 11a exhibits the AFM image of 30 nm pentacene film deposited on flexible substrate. Typical herringbone structure with feature size of ~ 2 μm can be clearly observed from left one in Figure 11a. In addition, in magnified image, terraces with height of ~ 1.5 nm can be clearly observed, as shown in the upper right one, corresponding to an edge-on configuration. To further explore the crystalline structure and molecular ordering of the deposited pentacene film, the corresponding GIXD pattern is recorded and the result is given in Figure 11b. As seen, the (001) reflection peak along the Q_z (out of plain) axis can be assigned to the "thin film phase" with a layer spacing of ~ 1.54 nm, which is approximately equal to the up-right standing molecular height [69]. Additionally, the {1, ±1}, {0, 2} and {1, ±2} in plane Bragg rod reflections at Q_{xy} (in plain) positions indicate that the pentacene crystal has a highly oriented 3D herringbone packing structure, as evidenced by many groups [69,70,71]. The "thin film phase" is believed to benefit the charge carrier transport, due to the preferred π-orbital overlap [72].

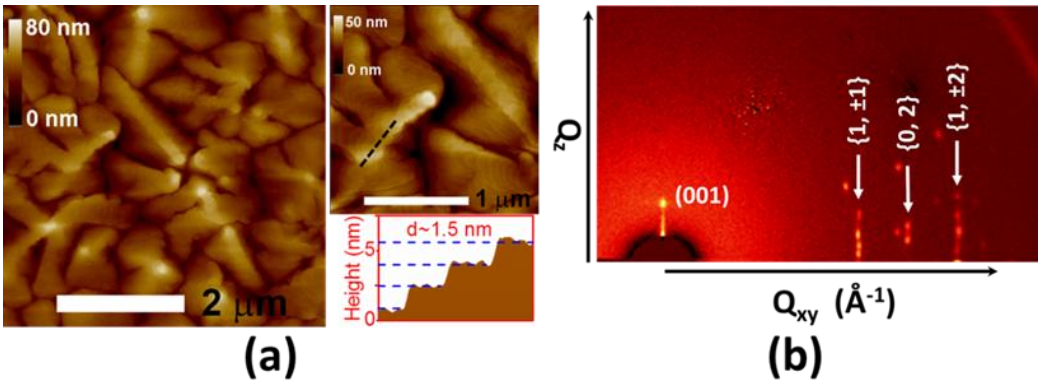

Figure 11. (a) AFM image of 30 nm pentacene film deposited on ODPA/ATO and the cross-sectional profile along the dark line; (b) the corresponding GIXD pattern.

We have proved the effectiveness of *M*-Cu as S/D electrodes in pentacene OTFTs. However, one major disadvantage of using Cu as S/D electrodes is the inevitable oxidation of Cu by oxygen species and water in air. To resolve this problem, a An encapsulation layer on *M*-Cu is employed.

Figure 12 shows the electrical characteristics of flexible pentacene TFT using 10 nm Au encapsulated 30 nm *M*-Cu (Au/*M*-Cu) as S/D electrodes. Due to the high capacitance density (180 nF/cm^2) of the ODPA/ATO system, the device can work perfectly under a low operating voltage of only −2 V. As shown in Figure 12a, the output curves exhibit distinct linear and saturation regions of a typical p-type feature, with a high saturation current on the order of 10^{-5} A under V_{GS} = V_{DS} = −2 V. No obvious leakage can be observed at zero V_{DS} due to the high quality of the ODPA/ATO system. Figure 12b plots the corresponding transfer curves in saturation region, from which the electronic parameters can be extracted. The device possesses outstanding electronic characteristics, with on/off ratio of 2 × 10^4, μ of 1.5 cm^2/Vs, V_T of −0.4 V and *SS* of 161 mV/dec. To the best of our knowledge, this obtained mobility value is among the highest ones achieved in flexible pentacene TFTs. The high performance of our flexible pentacene TFT with Au/*M*-Cu S/D electrodes can be ascribed to the "thin film pahse" of the deposited pentacene film and the potimized electrode/pentacene interface property.

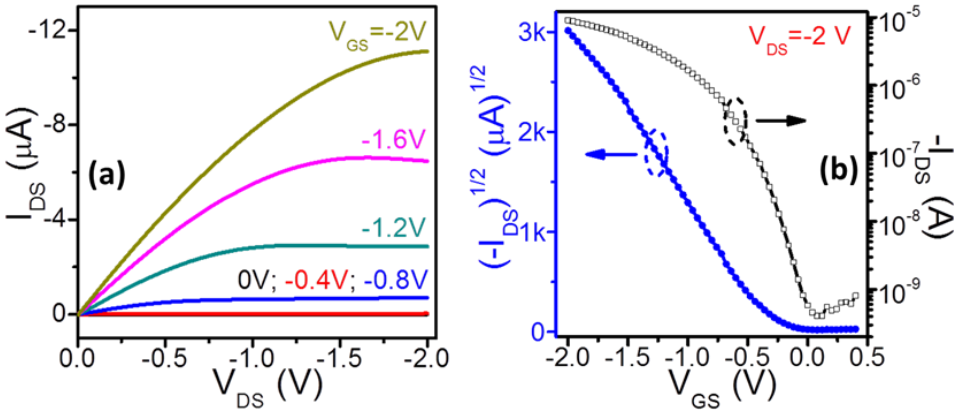

Figure 12. (a) Output and (b) transfer curves of flexible pentacene OTFT.

The mechanical flexibility of the devices is investigated at controlled bending radii along the channel length direction, under either compressive or tensile condition. Figure 13a and b show the relative variation in the normalized μ and V_T of the devices as a function of strain. As can be seen form Figure 13a, in case of compressive strains, the mobility decreases gradually with increasing the strain at first, and then a rapid degradation is observed. A 40% degradation in μ is observed at strain of 2.7%, and the V_T shifts in a small range from −0.55 V to −0.58 V. On the other hand, as shown in Figure 13b, in case of tensile strains, a more drastic degradation in the mobility is observed and only about 10% is preserved at strain of −2.7%, and the V_T shifts in a larger range from −0.46 V to −0.68 V. Yang et al. reported that the mechanical strain could induce phase transitions of pentacene between thin film phase and bulk phase [73]. To investigate the crystal structure variation, XRD patterns of 30 nm pentacene on flexible substrates are recorded under strains of ± 2.7%, and the results are shown in Figure 13c. For the as-deposited pentacene film, the only peak indexed as $(001)_T$ can be assigned to the thin film phase, with interlayer spacing of about 1.54 nm [74], which is in good agreement with the previous GIXD result. However, under both compressive and tensile strains, another peak shows up, which corresponds to the bulk phase of pentacene with interlayer spacing of 1.45 nm as denoted by $(001)_B$ in Figure 13c, indicating a phase transition occurs. Further investigations show that the mass fraction of the thin film phase is about 20% in compressive strain (2.7%), while about 14% in tensile strain (−2.7%). The remained higher thin film phase mass fraction

may partly account for the better mechanical flexibility of the OTFTs under compressive strains, since the bulk phase is reported to possess lower intrinsic mobility than the thin film phase [74].

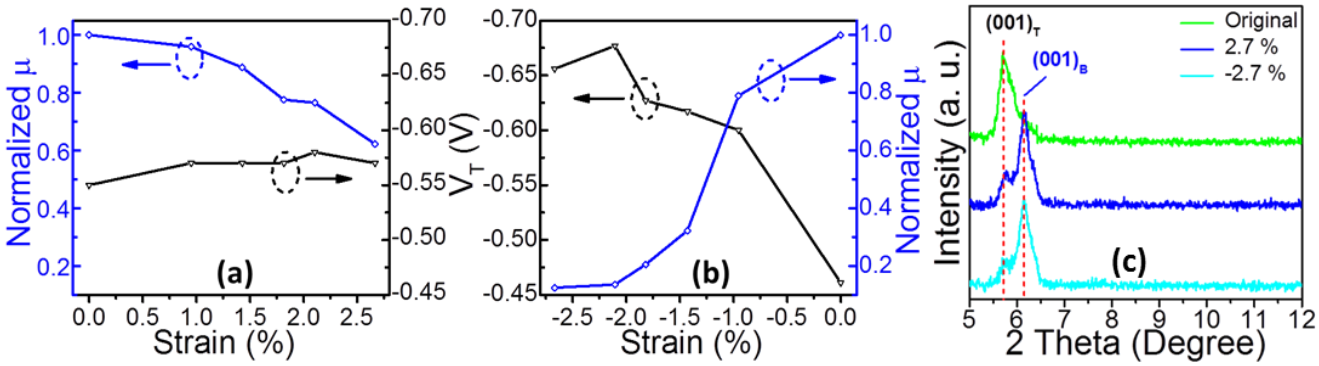

Figure 13. Relative changes in the normalized mobility of the flexible pentacene TFTs as a function of (a) compressive and (b) tensile strains; (c) XRD patterns of 30 nm pentacene film with different strains.

4. Conclusion

In summary, we have successfully achieved low-voltage OTFTs by introducing a solution-processed, low-temperature cured high-*k* ATO as the gate dielectric. The ATO based low-voltage CuPc OTFTs exhibit much higher device performance than the traditional 300 nm SiO_2 due to the difference in initial growth of CuPc. The electrical and physical-chemical performance of ATO can be optimized by ODPA modification, featuring in suppressed leakage and surface energy. By using interface engineering, highly improved electrical performance can be obtained in both pentacene and C_{60} OTFTs with low-cost *M*-Cu and Cu/PEI S/D electrodes at a low voltage. Furthermore, based on the above findings, flexible pentacene OTFTs with outstanding performance can be realized by employing ODPA/ATO as gate dielectric and Au encapsulated M-Cu as S/D electrodes. Our studies can further advance the development of large scale application of organic electronics featured with low-cost and low-voltage.

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Conflict of Interest

The authors report no conflict of interests in this research.

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