Research article

Analysis, design and performance evaluation of an LED driver with unity power factor and constant-current primary sensing regulation

Giovanni Gritti and Claudio Adragna*

Industrial & Power Conversion Division Application Laboratory—STMicroelectronics s.r.l.—via C. Olivetti 2—20864 Agrate Brianza (MB)—Italy

* Correspondence: Email: claudio.adragna@st.com; Tel: +390396035097; Fax: +390396035330.

Abstract: This work focuses on an isolated offline driver to power LED lamps, realized with a high-power-factor quasi-resonant (Hi-PF QR) flyback converter with peak current mode control and employing constant-current primary-sensing regulation (CC-PSR). The converter is controlled with a recently introduced control technique that enables this kind of converter to ideally draw a sinusoidal current from the input source and, at the same time, to accurately regulate the dc output current using only quantities available on the primary side. The resulting absence of an optocoupler or other means crossing the isolation barrier to close a feedback loop not only reduces size and cost of the driver but also brings greater safety and reliability. The analysis addresses those factors inherent in the control method that affect the shape of the input current that have not been covered in the existing literature. The aim is to set up some design guidelines to minimize the Total Harmonic Distortion (THD) of the input current. The experimental work shows that using this technique enables the design of an LED driver for wide range mains (90 to 264 Vac) that achieves output current regulation better than ±2%, power factor close to unity and THD of the input current <10% over the input voltage range and over a 2:1 range of the output voltage.

1. Introduction

The design of LED drivers is challenging in many respects [1]. For circuits supplied from the ac power line, the harmonic content of the ac input current is a relevant demanding aspect.

Due to the proliferation of LED lamps, the effect of low/medium power LED drivers on the electric power distribution line is a major concern [2–4]. For this reason, these systems must comply with the class C harmonic emission limits defined by the IEC61000-3-2 or other equivalent regulations. In addition, market requirements put considerable emphasis on the Total Harmonic Distortion (THD) of the ac input current: LED drivers are quite often specified to meet THD targets [5–9] that turn out to be more severe than the regulatory requirements of IEC61000-3-2 on the amplitude of the individual harmonics.

Standalone LED drivers (i.e., not embedded into a luminaire) are particularly challenging in this respect: they are often specified for a rated output current over a range of output voltages (a 2:1 range is quite typical) to power different types/lengths of LED strings. These devices must then comply with the IEC61000-3-2 and meet the THD targets even when operated at the specified minimum output voltage, which means at a fraction of their rated maximum power. To make things worse, in many cases light emission must be dimmable and/or drivers are specified to operate over a wide input voltage range (from 90 to 264 Vac). From the driver perspective, these features further extend the input voltage and the power range under consideration for THD targets.

From a different angle, LED drivers are a cost-sensitive application and quite a common way to help meet cost targets is to use the so-called constant-current primary sensing regulation (CC-PSR) technique. This configuration regulates the output dc current required for proper LED driving using only electrical quantities available on the primary side. In this way, the current sensing element, the voltage reference, the error amplifier on the secondary side and the optocoupler that transfers the error signal to the control circuit on the primary side are unnecessary. In addition to reducing the bill of materials and the required board space, this approach brings greater safety and reliability.

The high-power-factor (Hi-PF) flyback converter is perhaps the most popular topology used in low/medium power LED drivers supplied from the ac power line [10–25]. It meets the regulatory requirements on the power factor and the ac input current harmonic content, as well as those on safety isolation, with a simple and inexpensive power stage. Additionally, it lends itself to implementing CC-PSR in a relatively simple way and with good performance [15–22].

In many cases, Hi-PF flyback converters are operated with a fixed switching frequency and in the discontinuous conduction mode (FF-DCM) [10–18]. As taught in [26], this makes the flyback converter an ideal rectifier, theoretically able to provide unity power factor and zero THD.

Hi-PF flyback converters can also be operated in the so-called QR mode, i.e., synchronizing the beginning of switching cycles to transformer demagnetization. QR operation brings a few benefits as compared to FF-DCM: lower conducted EMI emissions, safer operation under short circuit conditions, valley-switching or even true soft-switching (zero-voltage switching, ZVS). However, its standard implementation (that can be found in a large number of commercial products primarily intended for boost PFC converters) provides a sinusoidal envelope of the peaks of the primary current. This cannot achieve a very low THD of the input current, as demonstrated in [19–25]. In these papers, various techniques to reduce the THD are reported. Though effective, none of them can theoretically provide unity power factor and zero THD like in a FF-DCM Hi-PF flyback converter.
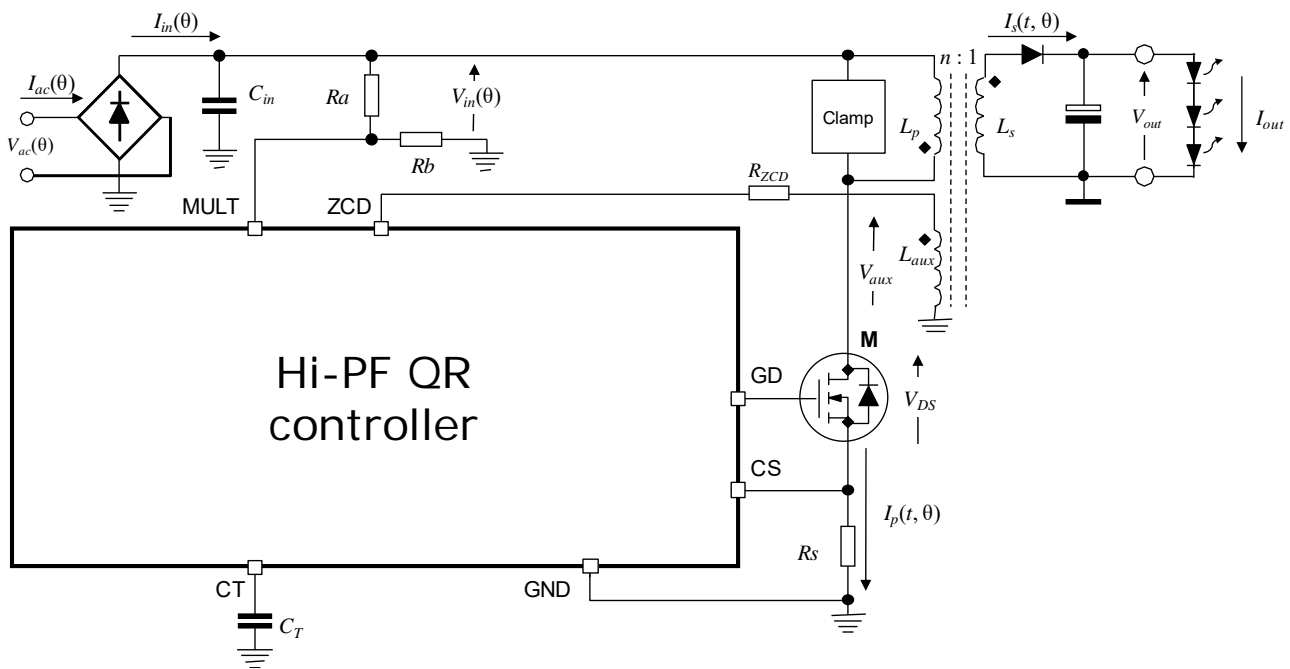
Figure 1. Principle schematic of an LED driver based on a Hi-PF QR flyback converter.

Relatively recently, a control method has been disclosed [27] that is able to provide Hi-PF QR flyback converters, whose basic circuit is shown in Figure 1, with the ability to ideally get a sinusoidal input current (unity power factor and zero THD like FF-DCM ones) and to perform CC-PSR. In this way, the combined benefits of QR operation and CC-PSR can be obtained with minimum penalty in terms of THD. The present work will take this method under consideration.

The analysis presented in the existing literature on this topic [27–28], however, does not fully explore the causes of distortion of the input current that are inherent in the control method. This will be the main focus of the present work, with the aim of providing some design guidelines to meet the THD design targets with less effort. Therefore, this paper is arranged as follows: in section 2 the method [27] is reviewed; section 3 reviews the basic assumptions underlying the method, deals with the causes of distortion of the input current not previously analyzed and provides a few design guidelines to achieve minimum THD of the input current; section 4 will show some experimental results that validate the analysis; section 5 provides the conclusions.

2. Review of the control method

The control method described in [27] is essentially the combination of the control scheme described in [28] that ideally achieves a sinusoidal input current in a Hi-PF QR flyback converter with secondary-side regulation, and that described in [29] that achieves CC-PSR in a traditionally controlled Hi-PF QR flyback converter. Figure 2 shows the principle schematic, Figure 3 its key waveforms.

Basically, with the first method the peaks of the primary current are enveloped by a properly shaped profile so that the average input current in a switching cycle tracks exactly the profile of the rectified input voltage. With the second method, the amplitude of the peaks is controlled in a way that the average output current on a line cycle time base is kept constant.

Figure 2. CC-PSR-controlled Hi-PF QR flyback converter with sinusoidal input current; internal details of the control circuit implementing the method described in [27] are shown.

Figure 3. Key waveforms of the circuit in Figure 2; switching cycle time scale (left); line cycle time scale (right).

Recalling [27], the rectified input current to the converter, $I_{in}(\theta)$, with $(0 < \theta < \pi)$, which is found by averaging the primary current over each switching cycle, has the following expression:

$$I_{in}(\theta) = \frac{1}{2} I_{pkp}(\theta) \frac{T_{ON}(\theta)}{T(\theta)} \tag{1}$$

The peak envelope of the primary current $I_{pkp}(\theta)$ is determined by the programmed current reference $Vcs_{REF}(\theta)$ through the current sensing resistors R_S:

$$I_{pkp}(\theta) = \frac{Vcs_{REF}(\theta)}{Rs} \tag{2}$$

Therefore, to achieve a sinusoidal ac input current $I_{ac}(\theta)$, with $(0 < \theta < 2\pi)$, which is the odd counterpart of $I_{in}(\theta)$, $Vcs_{REF}(\theta)$ must be of the following type:

$$Vcs_{REF}(\theta) = Vcs_x \sin\theta \frac{T(\theta)}{T_{ON}(\theta)} \tag{3}$$

With reference to the control circuit in Figure 2, $Vcs_{REF}(\theta)$ is the output of an analog divider where its input $A(\theta)$ can be identified as the output of the shaper circuit (composed by R_{t1}, C_{t1}, I_{ch1} and switch driven by the timing signal Q) needed to achieve the sinusoidal input current [28]; its input $B(\theta)$ signal can be considered constant and is generated (through R_T, C_T, I_{CH} and the transformer demagnetization FW timing signal) in a proper way to achieve output current regulation [29].

With the same assumptions as in [28], applying charge balance to C_{t1} the resulting $A(\theta)$ signal is:

$$A(\theta) = R_{t1} I_{ch1}(\theta) \frac{T(\theta)}{T_{ON}(\theta)} = R_{t1} g_{m1} K_p (V_{PK} \sin\theta) \frac{T(\theta)}{T_{ON}(\theta)} \tag{4}$$

where g_{m1} is the current-to-voltage gain of the current generator $I_{ch1}(\theta)$, V_{PK} the peak of the rectified line voltage $V_{in}(\theta)$ and K_p the divider ratio $R_b/(R_a + R_b)$. Applying charge balance to C_T and denoting with G_M the current-to-voltage gain of the current generator $I_{CH}(\theta)$, it is possible to find:

$$B(\theta) = G_M R_T g_{m1} R_{t1} K_p (V_{PK} \sin\theta) \frac{T_{FW}(\theta)}{T_{ON}(\theta)} \tag{5}$$

C_T is assumed to be large enough so that the ac component (at twice the line frequency f_L) of $B(\theta)$ is negligible with respect to its dc component B_0:

$$B_0 = \overline{B(\theta)} = \frac{1}{\pi} G_M R_T g_{m1} R_{t1} K_p V_{PK} \int_0^\pi \sin\theta \frac{T_{FW}(\theta)}{T_{ON}(\theta)} d\theta \tag{6}$$

Applying the voltage-second balance to the primary winding of the flyback transformer, the on-time $T_{ON}(\theta)$ of the power switch M and the secondary conduction time $T_{FW}(\theta)$ are related by the following relationship:

$$(V_{PK} \sin\theta) T_{ON}(\theta) = n (V_{out} + V_F) T_{FW}(\theta) = V_R T_{FW}(\theta) \tag{7}$$

Considering that $K_v = V_{PK}/V_R$, the ratio between the times $T_{FW}(\theta)$ and $T_{ON}(\theta)$ is:

$$\frac{T_{FW}(\theta)}{T_{ON}(\theta)} = K_v \sin\theta \tag{8}$$

The dc component B_0 of $B(\theta)$ is found by combining (8) and (6) and solving the integral:

$$B_0 = \frac{G_M R_T g_{m1} R_{t1} K_p V_{PK} K_v}{2} \tag{9}$$

Finally, the current reference $Vcs_{REF}(\theta)$, output of the divider A/B, is:

$$Vcs_{REF}(\theta) = K_D \frac{A(\theta)}{B(\theta)} \approx K_D \frac{A(\theta)}{B_0} = \frac{2K_D}{G_M R_T K_v} \sin\theta \frac{T(\theta)}{T_{ON}(\theta)} \tag{10}$$

where K_D is the divider gain (dimensionally a voltage).

Equation 10 has the same form as (3), with $Vcs_x = 2 K_D/(G_M R_T K_v)$, thus the control mechanism in Figure 2 shapes the rectified input current $I_{in}(\theta)$ as a rectified sinusoid and, then, the ac input current $I_{ac}(\theta)$ as a sinusoid. It is worth noticing that this result is achieved independently from the duration T_R of the time interval following transformer demagnetization (refer to Figure 3). The only constraint is that the converter does not operate in CCM (Continuous Conduction Mode).

The peak envelope of the secondary current $I_{pks}(\theta)$ can be calculated considering that the secondary current is $n = Np/Ns$ times the primary current $I_{pkp}(\theta)$, found by combining (10) and (2):

$$\begin{cases} I_{pkp}(\theta) = \dfrac{1}{R_S} \dfrac{2K_D}{G_M R_T K_v} \sin\theta \dfrac{T(\theta)}{T_{ON}(\theta)} \\ I_{pks}(\theta) = \dfrac{n}{R_S} \dfrac{2K_D}{G_M R_T K_v} \sin\theta \dfrac{T(\theta)}{T_{ON}(\theta)} \end{cases} \tag{11}$$

The average value in a switching cycle of the secondary current is:

$$I_o(\theta) = \frac{1}{2} I_{pks}(\theta) \frac{T_{FW}(\theta)}{T(\theta)} = \frac{1}{R_S} \frac{n K_D}{G_M R_T K_v} \sin\theta \frac{T_{FW}(\theta)}{T_{ON}(\theta)} \tag{12}$$

and the dc output current I_{out} is the average of $I_o(\theta)$ over a line half-cycle:

$$I_{out} = \overline{I_o(\theta)} = \frac{1}{\pi} \int_0^\pi \frac{n K_D}{G_M R_T K_v R_S} \sin\theta \frac{T_{FW}(\theta)}{T_{ON}(\theta)} d\theta \tag{13}$$

Finally, combining (13) and (8) and solving the integral the average output current is given by:

$$I_{out} = \frac{n K_D}{2 G_M R_T R_S} \tag{14}$$

which shows that the regulated dc output current I_{out} depends solely on external, user-selectable parameters (n, Rs) and on internally fixed parameters (G_M, R_T, K_D). It does not depend on the output voltage V_{out}, nor on the rms input voltage V_{in} or the switching frequency $f_{SW}(\theta) = 1/T(\theta)$.

Therefore, the control circuit shown in Figure 2, in addition to providing ideally unity power factor and zero harmonic distortion of the ac input current (PF = 1 and THD = 0), performs CC-PSR as well, i.e., it provides a regulated output current using only quantities available on the primary side, without any dedicated circuitry on the secondary side.

It is worth noticing that also the ability to perform CC-PSR is constrained to the converter not operating in CCM.

3. Discussion of the control method

In this section the discussion will be focused on the sinusoidal shaping of the input current operated by the control method analyzed in the previous section. As highlighted in [27–29], this analysis is based on some fundamental assumptions. Specifically:

1. The converter is operated so that the power switch M is turned on in each cycle after the secondary current reaches zero, therefore in QR-mode (i.e., on the first valley of the ringing that follows secondary current zeroing) or DCM (Discontinuous Conduction Mode).
2. The line voltage is sinusoidal, the input bridge rectifier is ideal, the voltage drop across the power switch M in the ON-state is negligible and there is negligible energy accumulation on the dc side of the bridge, thus the voltage $V_{in}(\theta)$, sensed by the (R_a, R_b) divider and used as a 'template' for the input current shape, is a rectified sinusoid.
3. The transformer's windings are perfectly coupled (no leakage inductance), so that the energy stored in the primary winding is instantaneously transferred to the secondary winding; further, the turn-off transient of the power switch M has negligible duration. As a result, T_{FW} immediately follows T_{ON}.

In addition, achieving a sinusoidal shape of $I_{ac}(\theta)$ is based on the following assumptions inherent in (1) and (10) respectively:

4. During the time interval T_R elapsing from the instant when the transformer demagnetizes to the instant when the power switch M is turned on, the transformer current is constantly zero; consequently, the current in the instant when M is turned on is zero too (Zero-current switching at turn-on, ZCS).
5. the ac component (at twice the line frequency f_L) of the control voltage $B(\theta)$ is negligible with respect to its dc component B_0, like in any high-PF converter;

Assumption 1 is actually a constraint, already discussed in [28]: if not met, the system will not operate as expected. The other assumptions are approximations that simplify the analysis and, as such, may lead to overlooking phenomena that cause distortion of the input current. Assumptions 2, 3 and 4 actually concern the power processing mechanism of the Hi-PF QR flyback converter and their impact on the distortion of the input current will be addressed in another paper.

In this section the focus is on the causes of distortion ascribable to the control method. Some of them (switching frequency voltage ripple across the shaping capacitor C_{t1}, actual low-frequency shape of the reference generated across C_{t1} and propagation delay on the current sense path) have been analyzed in [28] already and will not be treated here. The discussion in this section will concentrate on the implications of assumption 5, which is crucial for the selection of the capacitor C_T (a selection criterion is missing so far); additionally, the effects of the input offset voltage of the PWM comparator (see Figure 2) will be investigated with the aim of providing a design criterion to the IC designer.

3.1. Distortion caused by the low frequency ripple of the control voltage $B(\theta)$

The ac component at $2f_L$ of the control voltage $B(\theta)$, though small as compared to its dc component B_0, is a source of distortion inherent in the control method. To evaluate its impact, it is convenient to rewrite (5) taking (8) into account and simplifying the notation:

$$B(\theta) = \Gamma \sin^2\theta = \frac{\Gamma}{2}(1 - \cos 2\theta) \tag{15}$$

It is easy to recognize that $\Gamma/2 = B_0$. This equation is the result of averaging over a switching cycle; in other words, it expresses the voltage that would be developed across the resistor R_T if the C_T capacitor (see Figure 2) was just large enough to make the ac component at the switching frequency negligible. However, in order for assumption 5 to be valid, C_T must be much bigger, in order to keep the ac component at $2f_L$ low as well.

It is possible to think that $B(\theta)$ given by (15) is obtained by an equivalent current generator $B(\theta)/R_T$, whose dc and ac component are both equal to $\Gamma/2R_T = B_0/R_T$. As we consider a large capacitor C_T in parallel to R_T, so that its reactance X_T at $f = 2f_L$ is much smaller than R_T, the dc component B_0/R_T develops the dc voltage B_0 while the ac component B_0/R_T generates an ac voltage in quadrature (lagging) whose peak amplitude B_{acpk} is equal to $B_0 X_T/R_T$:

$$B(\theta) = B_0 \left(1 - \frac{1}{4\pi f_L R_T C_T} \sin 2\theta \right) \tag{16}$$

Substituting this expression in (10) and taking (2) into account, (1) can be rewritten as:

$$I_{in}(\theta) = \frac{1}{2}\frac{Vcs_x}{Rs} \frac{\sin\theta}{1 - \frac{1}{4\pi f_L R_T C_T}\sin 2\theta} \tag{17}$$

$I_{ac}(\theta)$ is given by (17) too, simply considering $\theta \in (0, 2\pi)$.

The diagrams in Figure 4, left to right, show the shape of $I_{ac}(\theta)$ for increasing values of the quantity $(4\pi f_L R_T C_T)^{-1}$ i.e., for increasing amplitude of the low frequency ac component of $B(\theta)$ (compared to the dc value B_0). A dotted black sinusoid is shown too for reference.

A Fourier analysis of (17) shows that there is an additional small component at the fundamental frequency and that the distortion is nearly all concentrated on the third harmonic; the higher order odd harmonics (even harmonics are zero, being the function hemisymmetrical) become negligible very quickly, as depicted in the left-hand diagram of Figure 5.

The Fourier series expansion of (17) involves both sines and cosines, so that the odd harmonics are alternately in-phase and in quadrature with the fundamental. In particular, the fundamental leads $\sin(\theta)$ by few degrees and the third harmonic lags behind the fundamental by 90°.

The THD of the input current resulting from (17) is shown in the right-hand diagram of Figure 5 (red trace) along with its approximate expression (blue trace):

$$THD\% = \frac{50}{4\pi f_L R_T C_T} \tag{18}$$

which provides a simple and accurate relationship linking the amount of distortion generated by the

low-frequency ripple on the control voltage and the capacitor C_T. In fact, the error is <0.5% for values of $(4\pi f_L R_T C_T)^{-1}$ within 0.2 and <0.13% for values of $(4\pi f_L R_T C_T)^{-1}$ within 0.1.
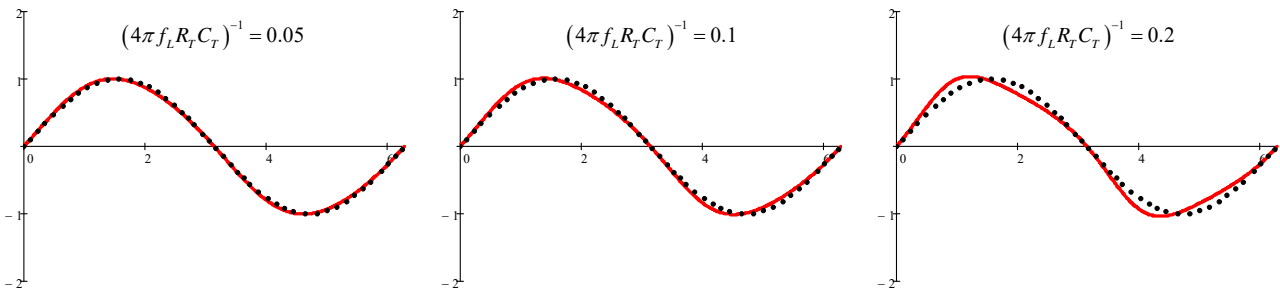

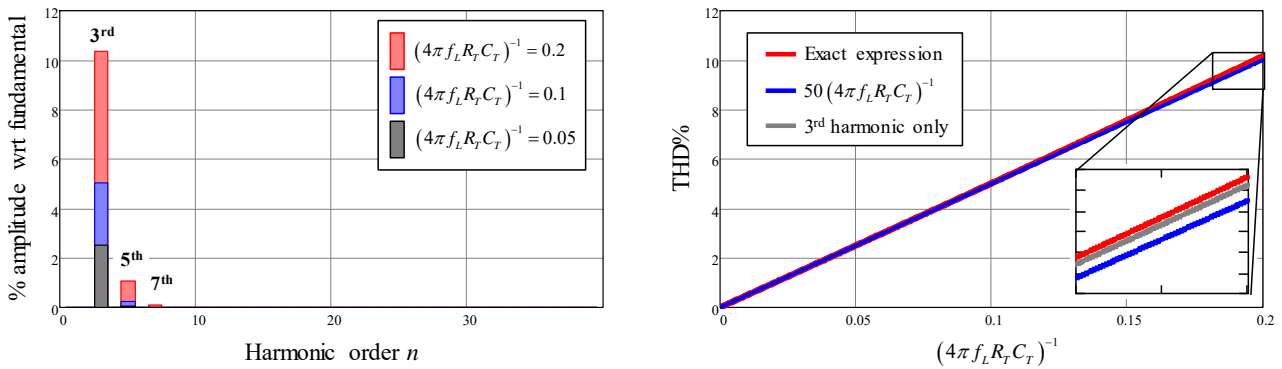**Figure 4.** Shape of $I_{ac}(\theta)$ given by (17) for different values of $(4\pi f_L R_T C_T)^{-1}$.

Figure 5. Harmonic contents of (17) for different values of $(4\pi f_L R_T C_T)^{-1}$ (left); THD of (17) and its approximation (18) as a function of $(4\pi f_L R_T C_T)^{-1}$ (right).

The plot on the right-hand side of Figure 5 shows also the 3rd harmonic (grey trace), visible in the zoomed window only, which is essentially overlapped to the THD plot, reiterating the dominance of the third harmonic: it accounts for 99.5% of THD at $(4\pi f_L R_T C_T)^{-1} = 0.2$ and for 99.9% of THD at $(4\pi f_L R_T C_T)^{-1} = 0.1$.

Notice that (18) can be rewritten as:

$$THD\% = 50 \frac{B_{ac_{pk}}}{B_0} \tag{19}$$

This is essentially equal to the expression of the third-harmonic distortion that can be found for multiplier-based power factor correction schemes [30]. This proves that using an analog divider instead of the multiplier does not bring any significant difference in terms of input current distortion as long as the peak amplitude of the ac component of $B(\theta)$, B_{acpk}, is sufficiently smaller than the dc component B_0. To confirm this statement from a different angle, it is possible to prove that, expanding (17) to Maclaurin series with respect to the variable $(4\pi f_L R_T C_T)^{-1}$, the first order term is exactly the same that is found in case of multiplier-based power factor correction schemes.

In principle, once specified the 3rd harmonic distortion budget allocated to the low-frequency ripple, either (18) or (19) enable the computation of the required C_T value. In section 4 a more practical design rule will be provided; based on that, the required C_T value can be computed with (16).

3.2. Effects of the input offset voltage of the PWM comparator

It is well-known that the input offset voltage of a comparator is the differential input voltage at which its output changes from one logic level to the other. It is most often caused by the mismatch of the transistors (either BJTs or FETs) in the input stage. These transistors should be relatively large to minimize the causes of mismatch but large transistors are slower (and more silicon consuming!) than small transistors. On the other hand, the PWM comparator (see Figure 2) must be fast to minimize the total propagation delay in the current sense path. For this reason, in commercially available control ICs the offset of the PWM comparator is the result of a trade-off.
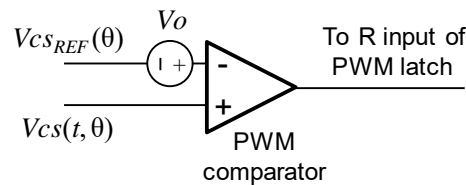

Figure 6. Symbolic representation of PWM comparator's input offset voltage.

Usually the offset is in the 10 mV range, a voltage level that in any PFC converter is found on the current sense input when the line voltage is around the zero crossings. It is therefore worth investigating its effect on the shape of the input current.

Input offset voltage is symbolically represented by a voltage source in series with either input terminal of the comparator. In our analysis it is convenient to consider this generator so that it adds up to the $Vcs_{REF}(\theta)$ signal, as shown in Figure 6. Notice that Vo can be either positive or negative. With this representation, the turn-off condition (2) of the power switch M can be rewritten as:

$$I_{pkp}(\theta) = \frac{Vcs_{REF}(\theta) + Vo}{Rs} \tag{20}$$

where $Vcs_{REF}(\theta)$ is still given by (3). This considering, (1) becomes:

$$I_{in}(\theta) = \frac{1}{2Rs}\left[Vcs_x \sin\theta + Vo\frac{T_{ON}(\theta)}{T(\theta)}\right] \tag{21}$$

The contribution of the input offset voltage, expressed by the term $Vo\,T_{ON}(\theta)/T(\theta)$ in (21), has a twofold effect: on the one hand it offsets (upwards or downwards, depending on the sign of Vo) the input current waveform, like with the traditional control technique, producing crossover distortion; on the other hand, since the actual offset is a function of the instantaneous line voltage (because of the term $T_{ON}(\theta)/T(\theta)$), the shape of the current is affected as well. The amount of distortion caused by the offset Vo depends on the ratio Vo/Vcs_x and a Fourier analysis of (21) shows that the distortion term creates a component at the fundamental frequency and odd harmonics, all in-phase (if $Vo > 0$) or

180° out of phase (if $Vo < 0$) with the fundamental component (no cosine term involved, then).

The diagrams of Figures 7 and 8 provide some exemplary quantitative results for the converter specified in Table 1, considering a positive and a negative offset respectively. The calculation method used to obtain these results is clarified in the appendix. The input offset is represented by the parameter $\rho = Vo/Vcs_{x\text{-}max}$, where $Vcs_{x\text{-}max}$ is the maximum value of $Vcs_x = 2\,K_D\,/(G_M\,R_T\,K_v)$, i.e., the one corresponding to the minimum value of K_v, $K_{v\text{-}min} = V_{PK\text{-}min}/V_R$).

Notice that in LED drivers specified to work in a certain range of output voltages V_{out} to power different types/lengths of LED strings, V_R is also variable, as stated by (7). Therefore, K_v is minimum at the upper end of the V_{out} range and maximum at the lower end of the V_{out} range. Notice also that in a CC-regulated converter a lower V_{out} (and V_R) means also a lower output (and input) power.
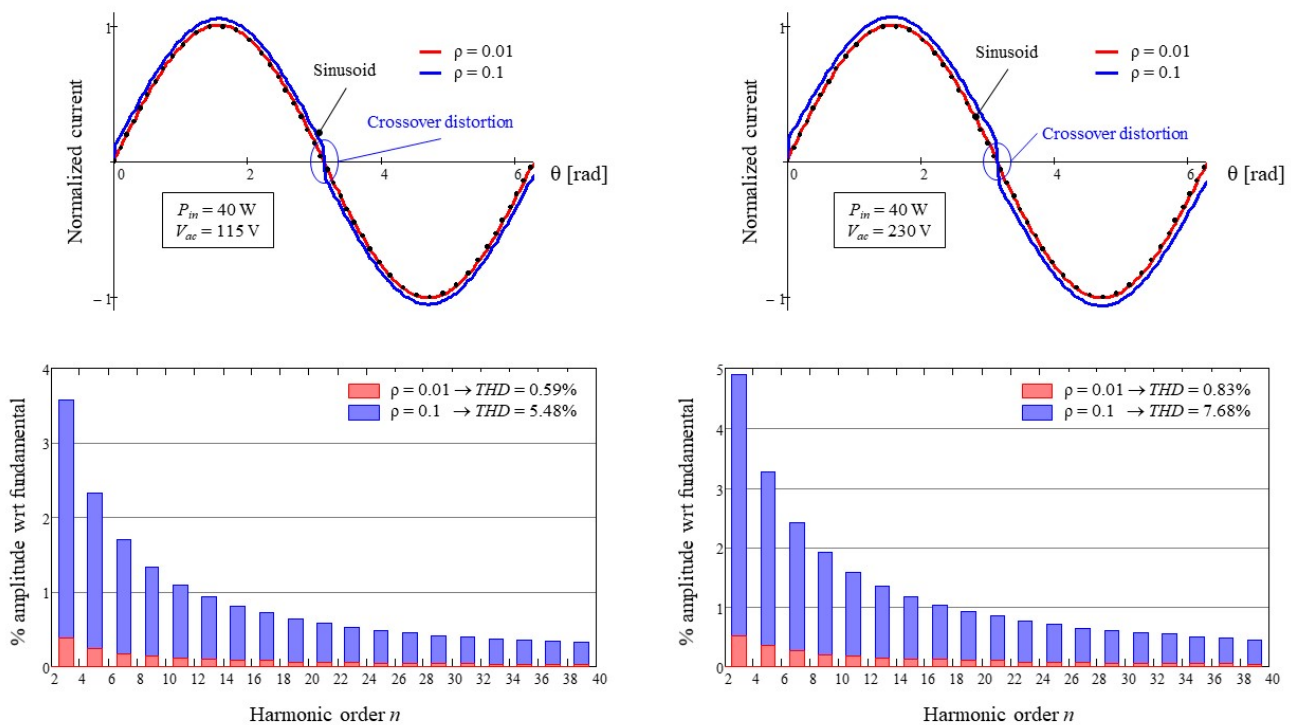

Figure 7. Effect of a positive input offset voltage of the PWM comparator: input current shape (upper) and its harmonic content (lower) for converter specified in Table 1 at 115 Vac (left) and 230 Vac (right).
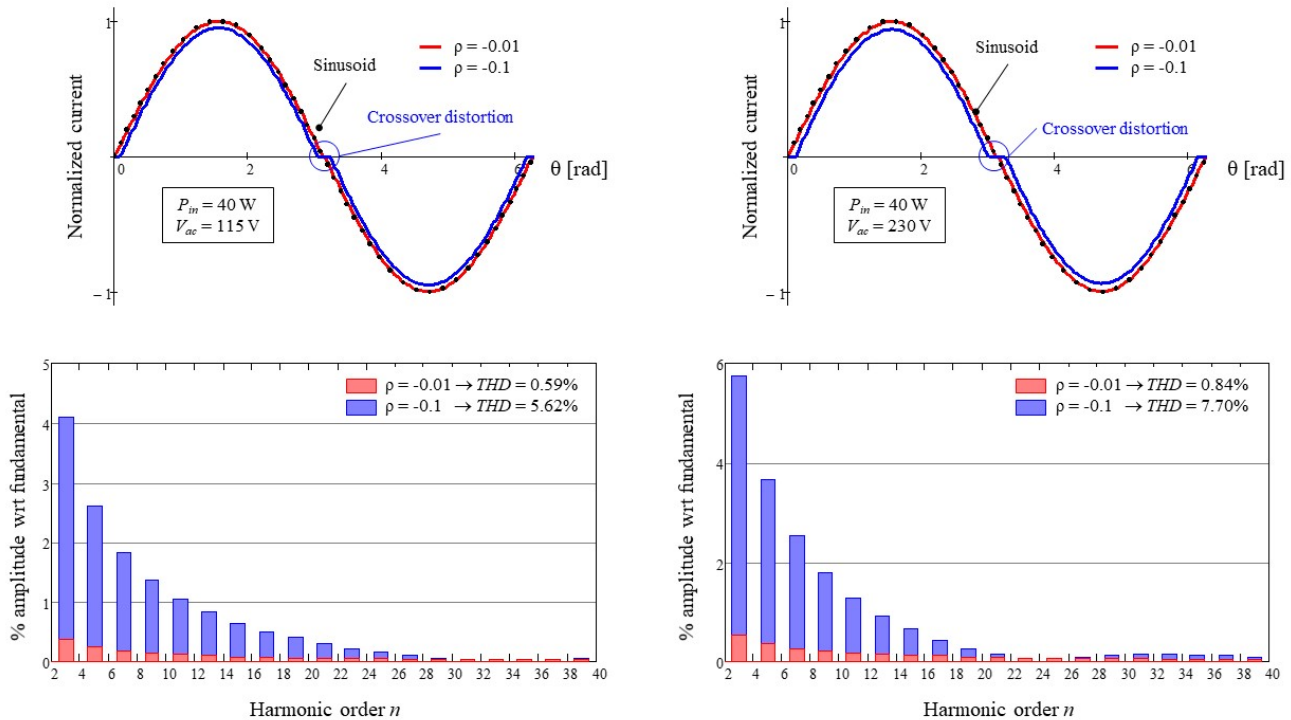
Figure 8. Effect of a negative input offset voltage of the PWM comparator: input current shape (upper) and its harmonic content (lower) for converter specified in Table 1 at 115 Vac (left) and 230 Vac (right).

Table 1. Main characteristics of the Hi-PF QR flyback converter used as a reference.

Parameter	Symbol	Value	Unit
Line voltage range	V_{acmin}-V_{acmax}	90–264	Vac
Line frequency range	f_l	47–63	Hz
Rated output voltage (14 LED string @ 100% load)	V_{out}	48	V
Regulated dc output current	I_{out}	700	mA
Expected full-load efficiency	η	84	%
Transformer primary inductance	L_p	500	μH
Reflected voltage	V_R	120	V
Drain node total capacitance	C_{DS}	150	pF

In both Figures 7 and 8, the diagrams on the left-hand side are relevant full load and V_{ac} = 115 V, those on the right-hand side are relevant to full load and V_{ac} = 230 V. The upper diagrams show the shape of the ac input current to the converter $I_{ac}(\theta)$ for two different values of ρ:ρ = 0.01 is realistic, ρ = 0.1 is exaggerated but has been considered to show more clearly the distortion caused. Currents are normalized to their peak value. A dotted black sinusoid is shown too for reference. The lower diagrams show the harmonic contents of the current waveforms in the upper diagrams.

Notice in Figure 7 that the shape of $I_{ac}(\theta)$ shows a little crossover distortion, highlighted by the blue circle, i.e., a sort of step change in $I_{ac}(\theta)$ from positive to negative and vice versa at the zero crossings of the instantaneous line voltage $V_{ac}(\theta)$. This is due to the positive offset that keeps the average input current larger than zero even with an extremely small $V_{in}(\theta)$. This distortion is

essentially invisible for ρ = 0.01, quite conspicuous for ρ = 0.1 and this is confirmed by the harmonic contents of $I_{ac}(\theta)$ and the resulting values of THD.

In Figure 8, which refers to the case of a negative input offset voltage, the shape of $I_{ac}(\theta)$ shows a different type of crossover distortion, highlighted by the blue circle: a time interval around zero crossings of the instantaneous line voltage $V_{ac}(\theta)$ where $I_{ac}(\theta) = 0$, although $V_{ac}(\theta) \neq 0$.

This type of crossover distortion, often termed dead zone, occurs when the term in brackets in (21) is negative. The physical interpretation of being $I_{in}(\theta) < 0$ and $I_{ac}(\theta) = 0$ around zero-crossings is that a negative $I_{in}(\theta)$ actually charges back the input capacitor (C_{in} in Figure 2) so that $V_{in}(\theta)$ becomes larger than $V_{ac}(\theta)$, the input bridge is reverse-biased and, consequently, $I_{ac}(\theta)$ is zero. Also in this case the distortion is negligible for ρ = 0.01 and conspicuous for ρ = 0.1. The harmonic contents and THD values are only slightly larger than in the case of positive offset, hence one could conclude that, apart from the different shape, a positive offset or a negative offset are essentially equivalent in terms of input current shape degradation.

However, there are very good reasons that make a positive offset preferable to a negative one. There are a number of phenomena related to the power processing mechanism of Hi-PF QR flyback converters, specifically those neglected by the previously mentioned simplifying assumptions 2, 3 and 4, that produce a dead zone in the ac input current $I_{ac}(\theta)$ like a negative offset. An additional negative offset would then exacerbate these phenomena, whereas a positive offset counteracts them and mitigates their effect.

The solutions described in [30], where these phenomena are described with reference to boost topology, are based on this concept.

As a conclusion, it is possible to state that as long as input offset voltage *Vo* is in the range of 1% of the dynamics of the current sense input, its contribution to the THD of the input current is extremely limited (well below 1%). Normally, the dynamics of the current sense input is dictated by considerations about the power dissipation on the sense resistor *Rs*, and the offset should be designed consequently. Conversely, if for any reasons the PWM comparator can be built with a given maximum *Vo*, say 10 mV, the dynamics of the current sense input should not be much lower than 1 V.

4. Experimental verifications

A prototype of an LED driver, shown in Figure 9 on the left-hand side and based on the reference Hi-PF QR flyback converter specified in Table 1, has been built and its performance evaluated on the bench. The control method reviewed in section 2 has been implemented in a test chip, shown in Figure 9 on the right-hand side, using STMicroelectronics' BCD6s (0.32 μm) technology.

Figures 10 to 12 summarize the salient results of this evaluation.

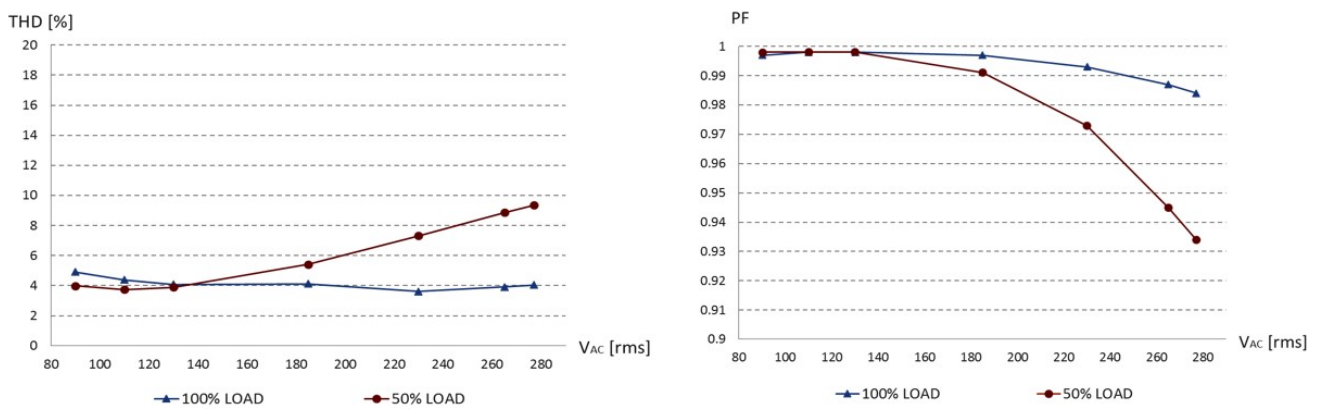**Figure 9.** LED driver prototype (left); control IC layout (right).

Figure 10. Experimental results: THD of the input current vs. V_{ac} (left) and PF vs. V_{ac} (right).
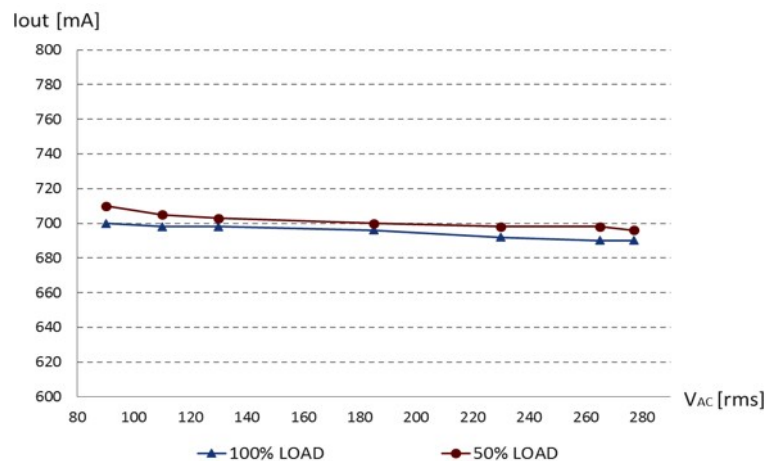

Figure 11. Experimental results: LED current regulation (CC-PSR accuracy).

Figure 10 shows the values of THD and PF achieved under different loading conditions over the full input voltage range. The THD is around 4% over the input voltage range. At 50% load (same output current, half the output voltage) it is still close to 4% at low line and increases at high line,

reaching 7.3% at 230 Vac and remaining below 10% at the upper end of the operating range. The PF is greater than 0.98 over the input voltage range at 100% load; at 50% load, at low line it is nearly equal to that at 100% load, at high line it drops to about 0.97 at 230 Vac.

The plot of Figure 11 shows the output current regulation versus ac line voltage (i.e., the dc current delivered to the LED string), for different LED string voltages. The regulated output current I_{out}, determined by the CC-PSR mechanism, lies in a band of ±10 mA centered on the target setpoint (700 mA, therefore ±1.4%), over the ac line voltage range and from 50% to 100% load. For a fixed load, the regulation band is approximately half as much. These measurements prove the very good accuracy of the CC-PSR regulation algorithm.

The experimental waveforms in Figure 12 show a shape if $I_{ac}(\theta)$ that is very close to an ideal sinusoid at full load both at 115 Vac and 230 Vac. At half load and 115 Vac the waveform is still very close to a sinusoid, whereas at 230 Vac the distortion, though low, is clearly visible. Notice that at full load and 115 Vac $I_{ac}(\theta)$ shows spikes at the zero crossings. These are due to the low frequency operation of the converter that comes close to the resonance frequency of the EMI filter. However, the harmonic contribution of these spikes are confined in the high frequency region, typically above the 40th harmonic considered by the regulations on harmonic current emissions (e.g., IEC61000-3-2).

Next, the dependence of the THD of $I_{ac}(\theta)$ on the value of the capacitor C_T was explored.

All the data and waveforms shown in Figures 10 to 12 are taken with C_T = 330 nF. In the control IC it is R_T = 120 kΩ, then $(4\pi f_L \, R_T \, C_T)^{-1}$ = 0.04 with f_L = 50 Hz (this line frequency has been used throughout all measurements); the value of C_T was swept in the range from 330 nF down to 22 nF, so that $(4\pi f_L \, R_T \, C_T)^{-1}$ changed in the range 0.04 to 0.603, and the value of THD measured at full load and different input voltages. The results are summarized in the plot of Figure 13.
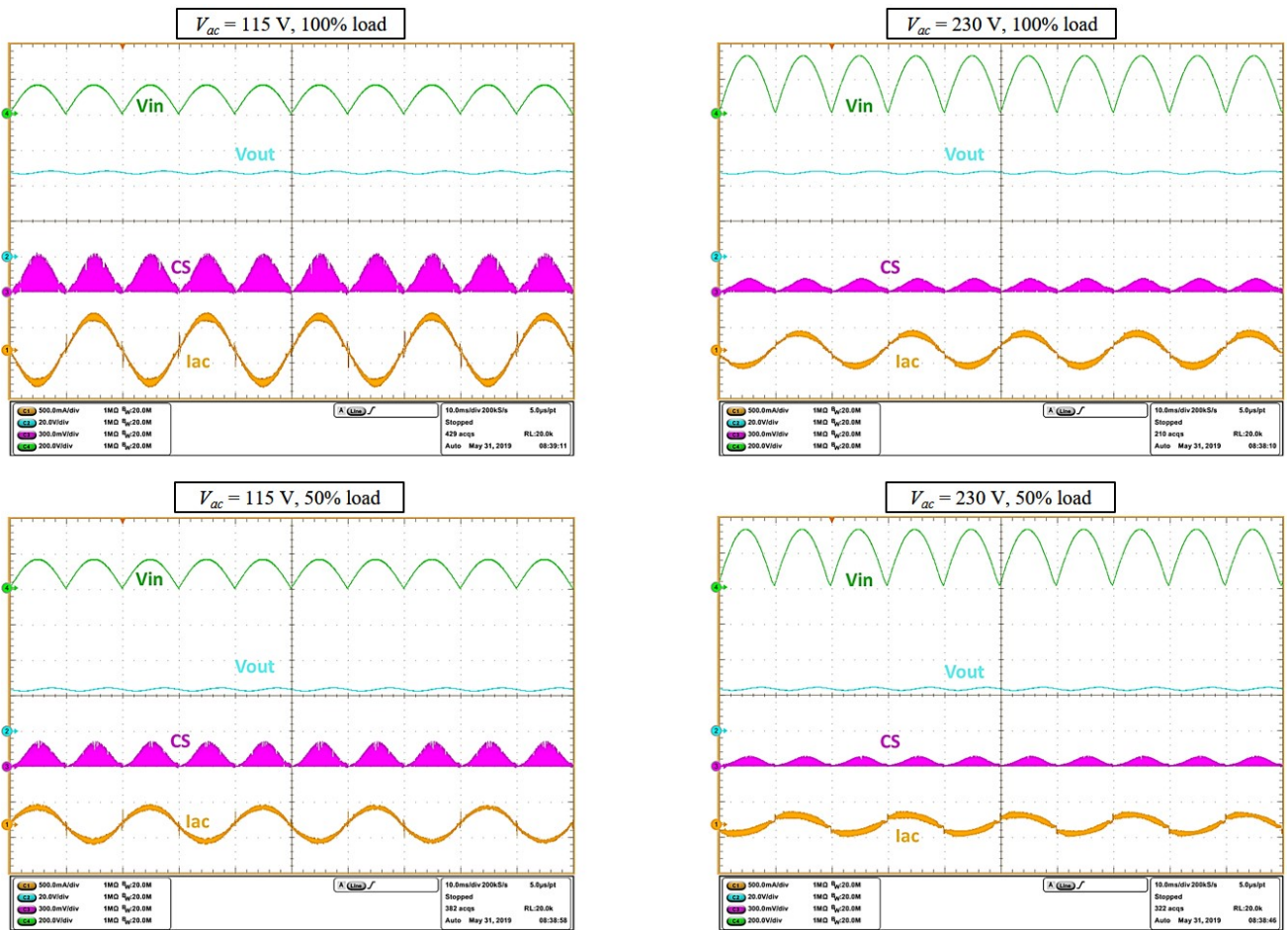
Figure 12. Experimental waveforms: V_{in}, V_{out}, Vcs, I_{ac} at 115 Vac (left-hand column) and 230 Vac (right-hand column), at full load (upper row) and half load (lower row).
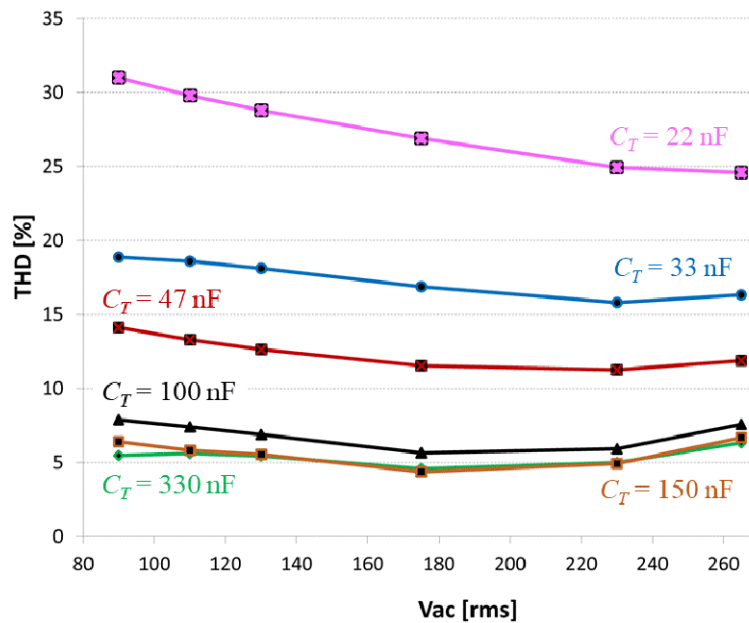

Figure 13. Experimental results: THD of the input current at full load vs. C_T.
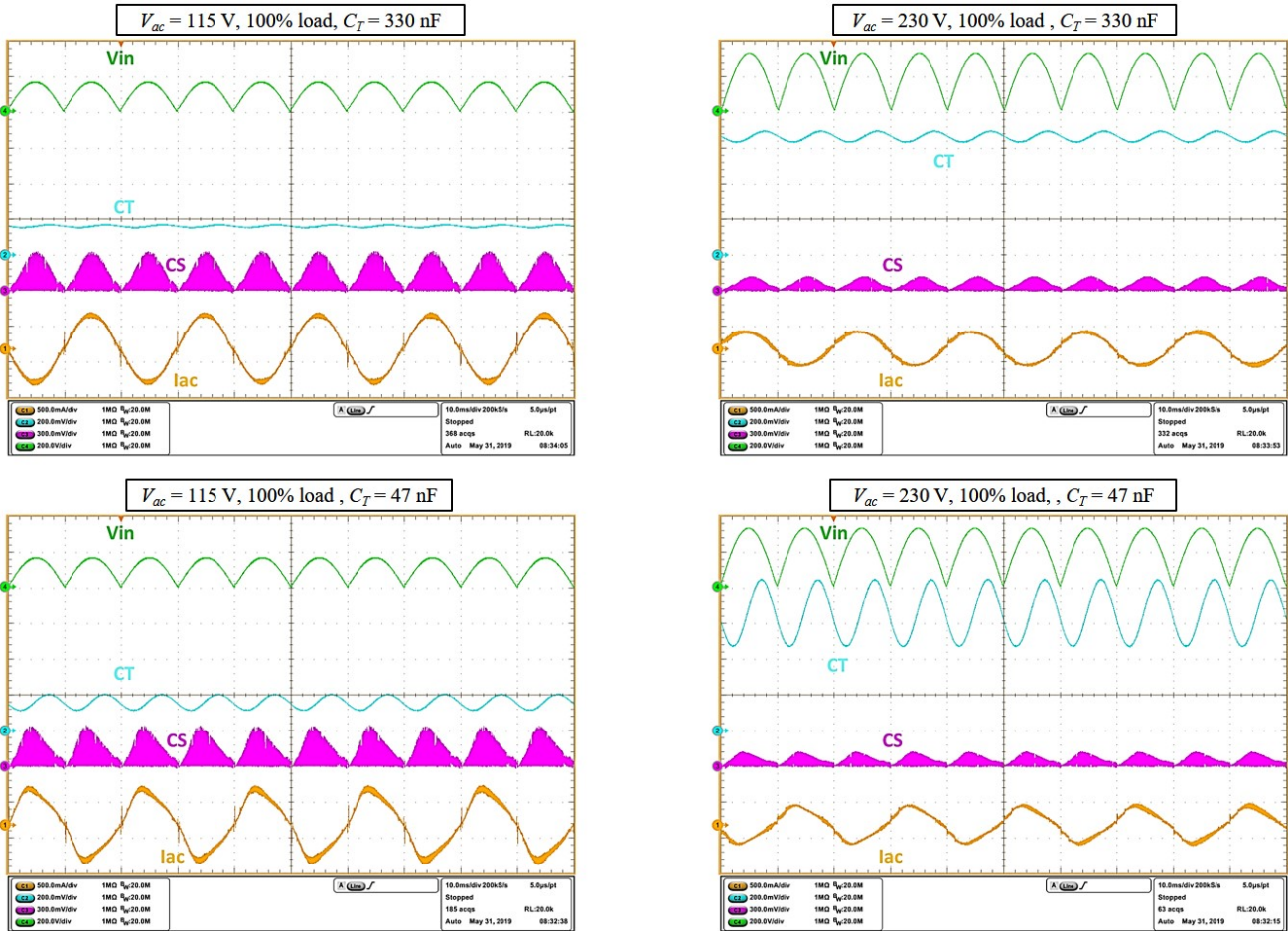
Figure 14. Experimental waveforms: V_{in}, $V(C_T)$, V_{cs}, I_{ac} at full load, 115 Vac (left-hand column), 230 Vac (right-hand column), with C_T = 330 nF (upper row), C_T = 47 nF (lower row).

The results obtained with C_T = 150 nF, corresponding to $(4\pi f_L R_T C_T)^{-1}$ = 0.088, are essentially coincident with those with C_T = 330 nF, except at 90 Vac where the THD is about 1% higher.

With C_T = 100 nF, i.e., $(4\pi f_L R_T C_T)^{-1}$ = 0.133, THD values increase by about 1–1.5% over those with C_T = 150 nF, still remaining well below 10% over the input voltage range. Significant degradation of THD can be observed with C_T values of 47 nF, corresponding to $(4\pi f_L R_T C_T)^{-1}$ = 0.282, and below. The experimental waveforms in Figure 14 refer to this condition.

From these results it is possible to conclude that, as long as $(4\pi f_L R_T C_T)^{-1}$ < 0.1, the THD of $I_{ac}(\theta)$ does not change much with C_T (its tolerance, as well as that of R_T, has little effect, then); additionally, there is no significant benefit in going below $(4\pi f_L R_T C_T)^{-1}$ < 0.05; rather, since this involves larger C_T values and the larger C_T is, the slower is the response of the CC-PSR loop to line and load changes, a design target of $(4\pi f_L R_T C_T)^{-1}$ = 0.1 seems an educated choice.

In other words, considering (16), the system designer should target a peak amplitude of the ac ripple of $B(\theta)$, B_{acpk}, equal to 10% of its dc value B_0, i.e., $(4\pi f_L R_T C_T)^{-1} \leq 0.1$. Since it is R_T = 120 kΩ, the value of C_T can be easily derived. Then, THD performance and dynamic performance can be traded off against one another to find the overall optimum operation with a series of bench tests.

5. Conclusions

The control methodology proposed in [27] that enables Hi-PF QR flyback converters with peak current mode control to ideally draw a sinusoidal current from the input source while regulating the output current using only quantities available on the primary side of the converter has been reviewed. After explaining the operating principle, the fundamental equations describing its operation have been recalled. A noticeable characteristic of the methodology emerging from this review is its user-friendliness: only two external parts are needed to set up a converter: a capacitor (C_T) to optimize the ac input current shape, and a resistor (Rs) to set the regulated output current.

The subsequent discussion has been concentrated on the effects of some significant nonidealities that in the real-world operation adversely affect the THD of the input current that were not previously analyzed. Specifically, the effects of the low frequency ac ripple on the control voltage of the CC-PSR loop (which the selection of the tuning element C_T depends on) and of the input voltage offset of the PWM comparator have been addressed.

The result of this analysis, corroborated by the experiments carried out on a prototype of an exemplary LED driver based on a control IC that implements the methodology under discussion, can be synthesized in the following two points:

1. The IC designer should target a ratio between the input voltage offset Vo of the PWM comparator and the dynamics of the current sense signal Vcs_{x-max} not exceeding 1%. In most practical cases the value of Vcs_{x-max} is dictated by considerations on the power dissipation of the current sensing resistor Rs and the effort directed to keeping Vo within that limit. Ideally, measures should be taken to achieve an always positive Vo because this would mitigate the effects of other nonidealities present in the system.
2. The system designer should target a peak amplitude of the ac ripple in the control voltage $B(\theta)$, B_{acpk}, equal to 10% of its dc value B_0 as a starting point for experimental system optimization. Being the B_{acpk}/B_0 ratio equal to the quantity $(4\pi f_L R_T C_T)^{-1}$, this is done through a proper selection of the C_T capacitor. This choice typically ensures an acceptable THD level that is also little sensitive to the tolerance of C_T. The optimum value of C_T will be found experimentally trading off the THD performance against the dynamic performance in case of line/load changes.

Of course, in the design of an LED driver, there are additional design guidelines to be taken into consideration to optimize the THD of the input current throughout the operating range. As mentioned in the preliminary discussion of the control method, in addition to the nonidealities in the control there are nonidealities in the power processing mechanism of the Hi-PF QR flyback converter that cause distortion of the input current. The most significant ones are the negative current after demagnetization, the zero-current detection mechanism, the input capacitor after the bridge rectifier.

Their impact can be minimized with proper design choices, but this is the topic of a future work.

Appendixes: Calculation of PWM comparator's input offset voltage impact on THD of $I_{ac}(\theta)$.

Firstly, it is convenient to rewrite (21) as follows:

$$I_{in}(\theta) = \frac{Vcs_x}{2Rs}\left[sin\,\theta + \frac{Vo}{Vcs_x}\frac{T_{ON}(\theta)}{T(\theta)}\right] \tag{A1}$$

Introducing the parameter $\rho = Vo/Vcs_{x\text{-}max}$, and keeping in mind the definitions of Vcs_x, $Vcs_{x\text{-}max}$ given in section 3.2, (A1) can be expressed as:

$$I_{in}(\theta) = \frac{Vcs_x}{2Rs}\left[sin\,\theta + \rho\,\frac{K_v}{K_{v-min}}\,\frac{T_{ON}(\theta)}{T(\theta)} \right] \tag{A2}$$

It is now necessary to calculate the ratio $T_{ON}(\theta)/T(\theta)$. In [28] one can find an approximate expression of $T_{ON}(\theta)/T(\theta)$ that neglects the idle time T_R after transformer demagnetization and before the beginning of a new switching cycle (refer to Figure 3). Here we want to provide a more accurate expression that takes T_R into account and that is used to build the plots of Figures 7 and 8.

The basic definition of $T(\theta)$, $T(\theta) = T_{ON}(\theta) + T_{FW}(\theta) + T_R$, by virtue of (8) becomes:

$$T(\theta) = T_{ON}(\theta)(1 + K_v\,sin\,\theta) + T_R \tag{A3}$$

As demonstrated in [28], the quantity $T_{ON}^2(\theta)/T(\theta)$ is constant for assigned operating conditions and its value is:

$$\frac{T_{ON}^2(\theta)}{T(\theta)} = \frac{4L_p}{K_v^2 V_R^2}\,P_{in} \tag{A4}$$

By combining (A3) and (A4) it is possible to obtain the following quadratic equation in $T_{ON}(\theta)$:

$$T_{ON}^2(\theta) - \frac{4L_p P_{in}}{K_v^2 V_R^2}(1 + K_v\,sin\,\theta)T_{ON}(\theta) - \frac{4L_p P_{in}}{K_v^2 V_R^2}T_R = 0 \tag{A5}$$

The solution is:

$$T_{ON}(\theta) = \frac{2}{K_v V_R}\left\{ \frac{L_p P_{in}}{V_R}\frac{1 + K_v\,sin\,\theta}{K_v} + \sqrt{L_p P_{in}\left[\frac{L_p P_{in}}{V_R^2}\left(\frac{1 + K_v\,sin\,\theta}{K_v}\right)^2 + T_R \right]} \right\} \tag{A6}$$

Of course, $T(\theta)$ is obtained inserting (A6) in (A3), and the ratio $T_{ON}(\theta)/T(\theta)$ can be readily computed using Mathcad® or other similar calculation tool. It is possible to recognize that, if in (A6) we set $T_R = 0$, then we find again the expressions of $T_{ON}(\theta)$ and $T(\theta)$ provided in [28].

Conflict of interest

The author declares no conflicts of interest in this paper.

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