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Research article

Device performances and instabilities of the engineered active layer with different film thickness and composition ratios in amorphous InGaZnO thin film transistors

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Abstract: The device performances and instabilities of the engineered active layer with different film thickness and composition ratios in amorphous InGaZnO thin film transistor prepared by RF-sputtering have been investigated. The engineered active layer devices were composed of an In and Zn rich front layer with thickness of 10 nm and a Ga rich back layer with thickness from 20 to 30 nm. The device instabilities were investigated under positive bias stress (PBS), negative bias illumination stress (NBIS) and high V_{GS} and V_{DS} stress. The device performances and the stability have been enhanced in channel engineered active layer a-IGZO TFTs due to the combination of the high conductive channel with In and Zn rich front layer and the passivation effects with the Ga rich back layer. The concurrent device degradation mechanism is suggested to explain the more severe device degradation under high V_{GS} and V_{DS} stress than the device degradation under PBS.

1. Introduction

Due to their excellent electrical properties and many advantages in device fabrication, amorphous InGaZnO (a-IGZO) has been getting much attention for the application of display devices. A-IGZO TFTs are currently considered as very interesting platforms to build wearable sensing devices due to their insensitivity to bending, conformability to the human body and low processing

cost. Since the demonstration of a-IGZO TFTs by Nomura [1], many research groups have contributed to enhancing the device performances and stabilities.

Especially, the composition ratios of amorphous InGaZnO oxide semiconductors have been known to play the key roles in the device performances and instabilities. Due to the formation of shallow oxygen vacancies, the electron mobility and the electron concentrations are increased with the increase of In ratio in a-IGZO TFTs [2]. From experimental work on the effects of In ratio on solution-processes a-IGZO TFTs, the decreased grain size and surface roughness lead to decreased trap density [3]. On the one hand, the higher In ratio leads to the increase of the off current and thus serious degradation of the ON/OFF current ratio. From an extensive experimental study on the Zn ratio's effects on the a-IGZO TFTs' microstructure, it was unfolded that a-IGZO's microstructure was changed from amorphous to nanocrystalline and then to columnar ZnO as the Zn ratio increases [4]. According to the microcrystal structures' transition, the electron concentration was increased, but the mobility was abruptly decreased when the microstructure changed to the columnar structure. Since the presence of grain boundaries in the microstructure of a-IGZO TFTs is attributed to the high defect concentration, the determination of the optimum Zn ratio is important for the grain boundary-free uniform properties and thus the low trap densities. Unlikely the role of In ingredient, the strong binding of Ga with oxygen atoms suppresses the generation of oxygen vacancies and reduces the electron concentration [5]. With considering an acceptable carrier concentration for proper ON/OFF current ratio, near-zero turn-on-voltage, high mobility, and low trap density, many studies suggested the optimum ingredient ratio of In:Zn:Ga = 1:1:1 in the atomic ratio[5,6].

Since the active layer thickness can be an influential factor in electrical properties in a-IGZO TFTs, the dependency of threshold voltage, mobility, and drive current on the active layer thickness has been extensively studied [7,8]. Although there are controversial reports of the trap density increasing or decreasing with the active layer thickness, the device degradation is more significant with decreasing the active layer thickness [8–11].

As one way to enhance the device performances and stabilities of oxide semiconductor thin film transistors, the solution-based devices with multi-stacked active layers were suggested [12–14]. For the homo-stacked active layer, the dual-active channel layera-IGZO TFTs composed of a conductive front channel and a stable backchannel were suggested [15–16]. The In rich front layer plays the roles of electron concentration and mobility booster, whereas the Ga rich back layer strengthens the resistance to the device degradation under bias and light illumination stress [16]. Although much research on solution-based oxide semiconductor devices with multi-stacked active layer has been reported [12–14], the instabilities of a-IGZO TFTs prepared by sputtering dual targets with different composition ratios have not been extensively investigated yet. In our previous work on the channel engineered a-IGZO TFTs, the In rich front layer and the microwave annealing were effective in reducing the device degradation under PBS [16].

Although many works on the device instabilities according to the active layer thickness and composition layer have been reported, the analysis of the total trap density using the extraction of the activation energy has not been reported. There is no profound research on which one is significantly influenced by the device instability between the active layer thickness and the composition ratio. Although much research on the device instabilities under high V_{GS} and V_{DS} stress have been reported, the mechanism for the more significant degradation compared to PBS has not been investigated in depth.

In this study, the engineered active layer devices with different composition ratios and thickness

in a-IGZO TFT prepared by RF-sputtering are suggested to enhance the device performance and reduce the device instability. The active layers of a-IGZO TFTs are composed of two layers according to the different channel composition ratios and thicknesses. The device instabilities were investigated under PBS, NBIS, and high V_{GS} and V_{DS} stress.The more significant degradationunder high V_{GS} and V_{DS} stresshas been discussedaccording to the film thickness and composition ratios.

2. Device fabrication and measurement

As shown in Figure 1, the a-IGZO TFTs used in this work were fabricated using a bottom gate configuration. Four kinds of a-IGZO TFTs were fabricated according to the active layer thickness and each active layer's composition ratios. A 100 nm thick of SiO_2 was thermally grown on p-type silicon substrate for the gate insulator. Then the composition ratio of In:Ga:Zn in 1:1:1 atomic ratio with the thickness of 30 nm (Device A) and 40 nm (Device B) were deposited as a single-active layer using RF magnetron sputtering with an Ar flow rate of 30 sccm, a pressure of 6 mTorr, and a power of 100 W at room temperature. For the dual-active layer, the In and Zn rich layer of a composition ratio of In:Ga:Zn in 2:1:2 with thickness 10 nm was deposited for the front active layer using RF magnetron sputtering. In the next stage, the back active layers of a composition ratio of In:Ga:Zn in 1:1:1 with the thickness of 20 nm (Device C) and 30 nm (Device D) were deposited using RF magnetron sputtering. After defining the active layer using photolithography, a microwave thermal annealing for 2 min at a frequency of 2.45 GHz and microwave power of 500 W in an O_2 gas ambient was performed to remove the interfacial defects at the active layer/gate oxide and the bulk traps. Finally, a 150 nm-thick Tilayers were deposited and patterned as the source and drain electrodes. The fabricated devices with a width/length of 120/90 μm were split into four categories according to the different active layer thickness and composition ratios, as presented in Table 1. The electrical measurements were carried out using Agilent B1500A precision semiconductor parameter analyzer in a dark box to avoid external light and electrical noise. To evaluate the device degradation under light illumination, a tungsten halogen lamp ranging from 320–1100 nm wavelength was used as a light source. The intensity of light source without filtering calibrated by photometry was 0.2 mW/cm^2.
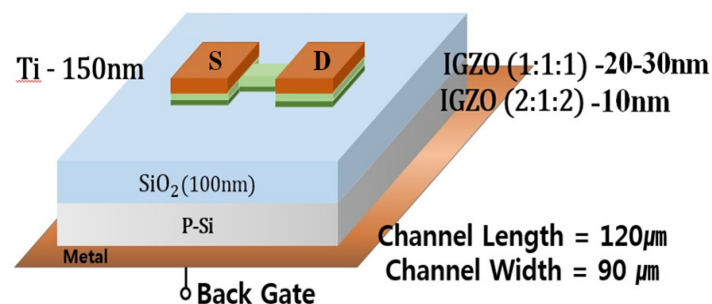

Figure 1. Schematic diagram of a fabricated a-IGZO TFT engineered active layer device.

Table 1. Device splits.

	Thickness and composition ratios
Device-A	30 nm (1:1:1)
Device-B	40 nm (1:1:1)
Device-C	10 nm (2:1:2) + 20 nm (1:1:1)
Device-D	10 nm (2:1:2) + 30 nm(1:1:1)

3. Results and discussion

Figure 2 shows the transfer characteristics of the fabricated four kinds of a-IGZO TFTs with different active thickness and composition ratios. The summary of the device performance parameters, including threshold voltage (V_{TH}), turn-on voltage (V_{ON}), field effect mobility (μ_{FE}), subthreshold slope (SS), and current ON/OFF ratio (I_{ON}/I_{OFF}) is presented in Table 2. The measured V_{TH} was defined as the V_{GS} corresponding to a constant drain current of 1*W/L (μA) at V_{DS} = 1.0 V, and μ_{FE} was extracted from the measured maximum transconductance. As one expects, V_{ON} and V_{TH} were decreased with the increase of the active layer thickness and the In ratios in both single and engineered active layer devices. The values of μ_{FE}, SS, and I_{ON}/I_{OFF} were enhanced in engineered active layer devices. Those indicate that there are no additional generations of interface defects in homo-stacked active layer devices. From the increase of I_{ON}/I_{OFF} in engineeredactive layer devices, the Ga rich back active layer with respect to the In rich front layer can be attributed to suppress the oxygen vacancies. From the comparison of device performance parameters between singleactive layer devices (Device A and B) and engineeredactive layer devices (Device C and D) with the same active layer thickness, significantly improved performances can be observed in engineeredactive layer devices. Therefore, one can suggest that the In rich front layer functions as the primary channel and the Ga rich back layer as the secondary channel in engineeredactive layer devices.
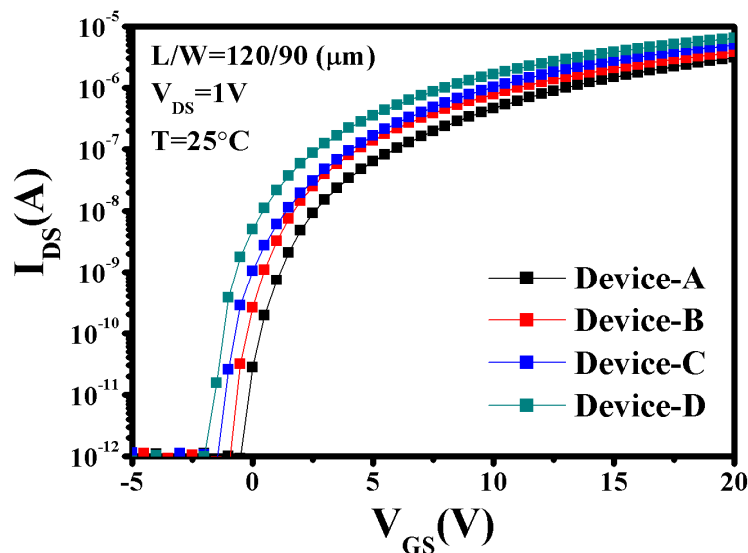

Figure 2. Transfer characteristics of single and engineeredactive layer devices with different layer thickness and composition ratios.

Table 2. Device electrical performance parameters.

Device	V_{TH} (V)	V_{ON} (V)	S.S. (V/dec.)	μ_{FE} (cm^2/V.S.)	I_{ON}/I_{OFF}
Device-A	2.589	0.154	0.73	5.54	1.02E + 06
Device-B	1.716	−0.389	0.68	6.27	1.38E + 06
Device-C	1.413	−0.861	0.57	7.86	1.85E + 06
Device-D	0.434	−1.315	0.52	8.35	2.47E + 06

For enhanced device performance in the engineered active layer device, the a-IGZO thin film's chemical states with different composition ratios have been examined using XPS. Figure 3 shows the O 1 s peak XP spectra of the a-IGZO according to the composition ratios of In:Ga:Zn in 1:1:1 and 2:1:2, respectively. The O 1 s peak was deconvoluted into three peaks at 531 eV, 532 eV, and 533 eV. The relative areas of the oxygen vacancies increase with the increase of In and Zn ratios. Therefore, the increasing of the relative concentration oxygen vacancies leads to the improved electrical properties of the a-IGZO thin film.
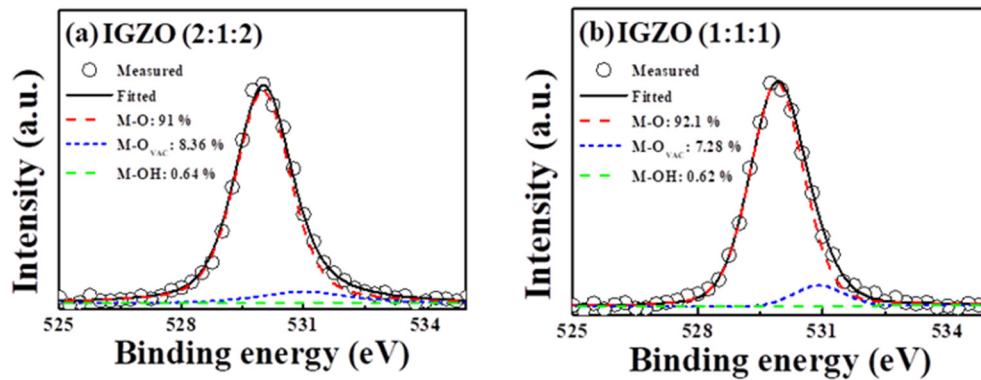

Figure 3. O 1 s Xp spectra of the a-IGZO thin film with different composition ratios for In:Ga:Zn = 2:1:2 (a) and 1:1:1 (b).

To further investigate the trap density including the interface traps and bulk traps, which influence the device instabilities, the conductance activation energy (E_a) was extracted from the temperature-dependent subthreshold currents as a function of V_{GS}. The subthreshold current is thermally activated and can be described using the following equation [17]

$$I_{DS} = I_{DS0} \cdot \exp(-E_a/kT) \tag{1}$$

where I_{DS0} is the prefactor and k is the Boltzmann constant. From the fitting of the temperature-dependent log (I_{DS}) versus 1/T curves in Eq 1, the $E_a = E_C − E_F$ (E_C and E_F are conduction band minimum and Fermi energy) were extracted as a function of V_{GS}. Figure 4 shows the E_a as a function of V_{GS}. E_a's falling rate with respect to V_{GS} in the subthreshold regime means E_F's change with respect to V_{GS} ($\partial E_F/\partial V_{GS}$). In the case of single active layer devices, the much faster falling rate of $\partial E_F/\partial V_{GS}$ in Device B compared to Device A means that the total trap density is reduced as the active layer thickness increases, which is in line with the previous report [8]. However, the opposite results were reported, in which the trap density was extracted from the SS measurement [10,18]. Since the extraction of the total trap density from SS measurement gives rise

to some deviations between the measured devices, the trap density from E_a extraction is believed to be more accurate than the one from SS measurement. E_a's much faster falling rate in devices C and D than A and B means that the total trap density is reduced in the engineeredactive layer for the same active layer thickness. Even though the acceptor like states could be increased with increasing In ratio [19], our results clearly show that the total trap density was reduced in engineeredactive layer devices. This may be attributed to the less interface trap density due to the reduced surface roughness when In and Zn ratios are increased [3–4]. The recent study revealed that the electrical properties and the stabilities have been improved when the grain boundary is free in IGZO thin film [20]. Therefore, the enhanced device performances can be attributed to the fewer grain binaries due to the reduced surface roughness with the increase of In and Zn ratio.
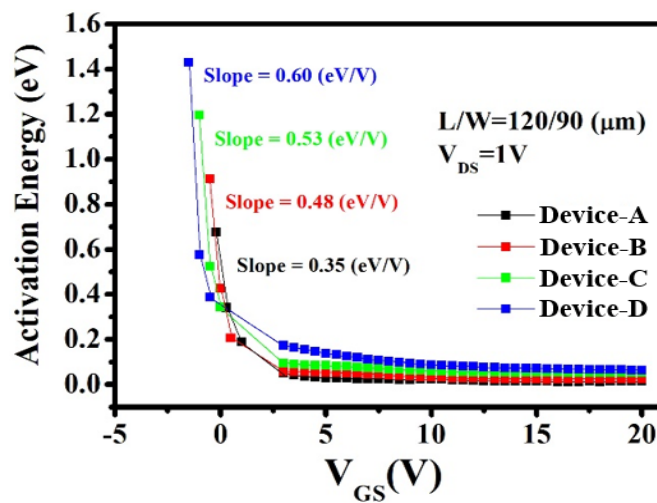

Figure 4. Variation of E_a as a function of V_{GS}.

The threshold voltage shifts (ΔV_{TH}) as a function of stress time under PBS at room temperature are presented in Figure 5. The devices were stressed under the conditions of $V_{GS} = 10$ V and $V_{DS} = 0$ V for 3600 s. In single active layer devices (Device A and B), the device degradation under PBS was decreased with increasing the active layer thickness. Although some previous reports argued that the thicker active layer contains more trap density [10,18], the more significant degradation in devices with a thinner active layer can be attributed to the more total trap density and the enhanced surface electric filed [21]. It is worth noting that the ΔV_{TH} of engineeredactive layer devices (Device C and D) are smaller than those of single active layer ones (Device A and B). Although the electron concentration in engineeredactive layer devices is larger than those of singleactive layer ones, the results above can be explained by a combinationof the passivation effects in the back secondary-active channel and the higher effective barrier height that the electron in the front primary-active channel can overcome into the gate oxide as our previous report [22]. The Ga rich back active layer compared to the front active layer reduces the absorption of O_2 from ambient and plays a role of the passivation effects. The In and Zn rich front active layer compared to the back active layer may reduce the surface roughness at the interface between the gate insulator and the active layer with the change of microstructure from amorphous to nanocrystalline [3–4], which leads to the higher effective barrier height between the gate insulator and the active front channel layer. This speculation is quite consistent with the aforementioned total trap density, extracted from the plot

of E_a versus V_{GS} as shown in Figure 4. Figure 6 shows the differences of PBS-induced ΔV_{TH_X} for different active layer thickness and single or engineeredactive layer. The ΔV_{TH_AB} and ΔV_{TH_CD} are attributed to the layer thickness difference, and the ΔV_{TH_AC} and ΔV_{TH_BD} are due to the single or engineeredactive layer's composition ratios. This result indicates that the composition ratios significantly influence the device degradation under PBS compared to the active layer thickness.
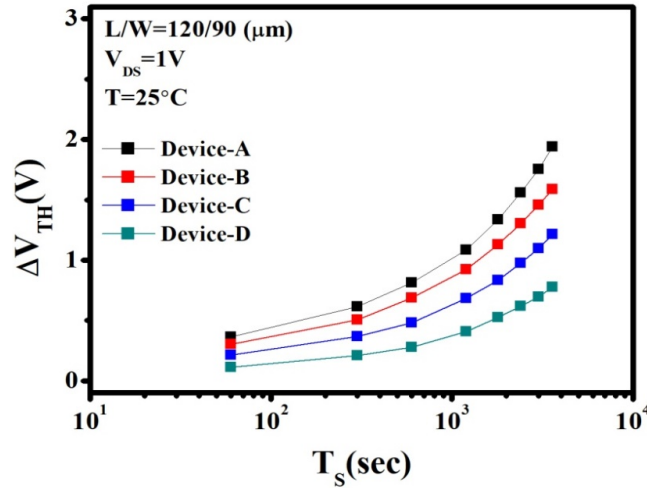

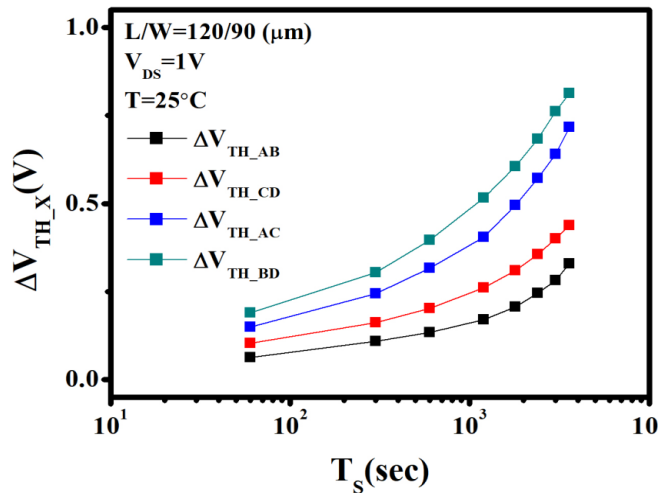**Figure 5.** ΔV_{TH} as a function of stress time under PBS at room temperature.

Figure 6. Difference of PBS-induced ΔV_{TH_X} for different active layer thickness and single or engineeredactive layer.

Figure 7 shows ΔV_{TH} as a function of stress time under NBIS. The devices were stressed under the conditions of $V_{GS} = -10V$ and $V_{DS} = 0$ V for 3600 s. In the case of single active layer devices (Device A and B), the NBIS-induced ΔV_{TH} in device with a thinner active layer was larger in magnitude than that with a thicker active layer. As previous reports [23], the device degradation under NBIS is increased due to the photo-generated electron-hole pairs and charged oxygen vacancies. In addition to the more trap density in devices with a thinner active layer, the more photo-generated holes have been trapped owing to the enhanced surface electric field [20]. One can

clearly observe that the ΔV_{TH} of engineeredactive layer devices (Device C and D) are smaller than those of singleactive layer ones (Device A and B). Since the bond dissociation energy is higher in GaO than InO, one can expect that the more photo-excited oxygen vacancies could be generated in engineeredactive layer devices compared to single active layer ones when the total thickness of the active layer is the same [24]. Therefore, NBIS-induced ΔV_{TH} in devices C and D with engineeredactive layer is expected to be larger than those of devices A and B. The opposite results can be explained by the combination of the passivation and the higher effective barrier height in engineeredactive layer devices as mentioned under PBS. The Ga rich back layer, which supresses the oxygen vacancy and leads to the electron concentration decrease, seems to passivate a secondary-active channel region. The In and Zn rich front layer which has an amorphous structure seems to increase the effective barrier height as in device degradation under PBS.
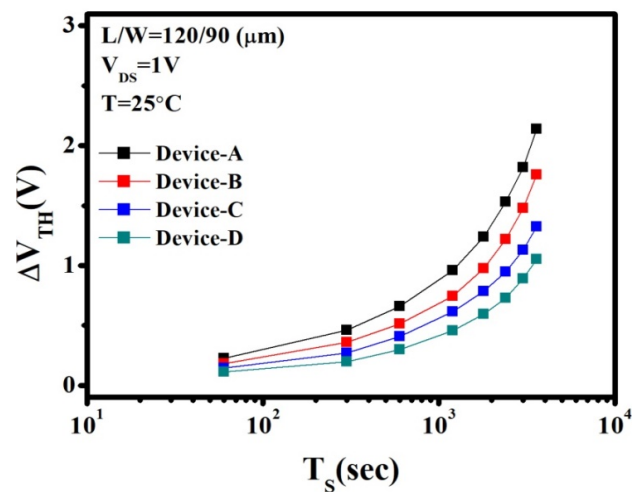

Figure 7. ΔV_{TH} as a function of stress time under NBIS.

Since the channel hot electrons are trapped in the bulk trap and/or at the interface states under high V_{GS} and V_{DS} stress, the device degradation is governed by the total trap density, the effective barrier height at the interface, the amount of the drain current, and the self-heating effect. The devices were stressed under the conditions of V_{GS} = 10 V and V_{DS} = 10 V for 3600 s. After high V_{GS} and V_{DS} stress, the transfer curves were shifted along the gate voltage axis in the positive direction and the drain currents were degraded. The evolutions of ΔV_{TH} as a function of stress time under high V_{GS} and V_{DS} stress, as shown in Figure 8, indicate that the ΔV_{TH} is dominated by negative trapped charges in bulk active layers or at the active channel interface and gate insulator, and by the generated acceptor-like states. In the case of single active layer devices, the ΔV_{TH} of thinner devices was larger in magnitude than that of thicker ones. Although the drain current of thicker devices leading to the more significant self-heating effect is larger than that of thinner ones, the more significant ΔV_{TH} of thinner devices can be attributed to a larger total trap density, which is quite consistent with the aforementioned in Figure 4. One can also observe that the ΔV_{TH} of engineeredactive layer devices is smaller than those of single active layer ones. From the transfer curves Figure 2, although the drain currents of engineeredactive layer devices are larger than that of singleactive layer ones, the less significant of ΔV_{TH} is attributed to a smaller trap density and the higher effective barrier height, especially due to the high In and Zn rich secondary active channel
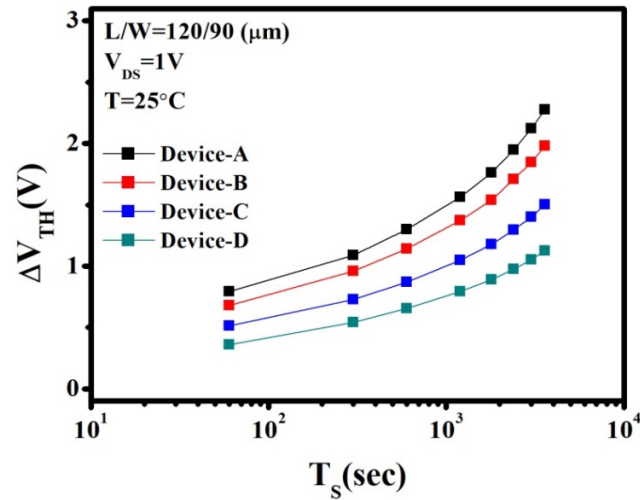
layer.

Figure 8. ΔV_{TH} as a function of stress time under high V_{GS} and V_{DS} stress.

The comparisons of ΔV_{TH} under PBS and high V_{GS} and V_{DS} stress were plotted for all tested devices in Figure 9. The ΔV_{TH} under high V_{GS} and V_{DS} stress are more severe threshold voltage instabilities than the ΔV_{TH} under PBS. According to many experimental works fitted with the device simulation including our study, the hot electrons caused by the large lateral electric field or self-heating effects can break the metal-oxygen bonds, thus generating defects such as donor-like shallow states or acceptor-like deep states [25–28]. There are still controversial reports on V_{TH}'s negative or positive shift after high V_{GS} and V_{DS} stress [25–28]. The balance between donor-like states and the trapped electron trapped charges as well as acceptor-like states is thus critical to affecting the direction of the V_{TH} shift.
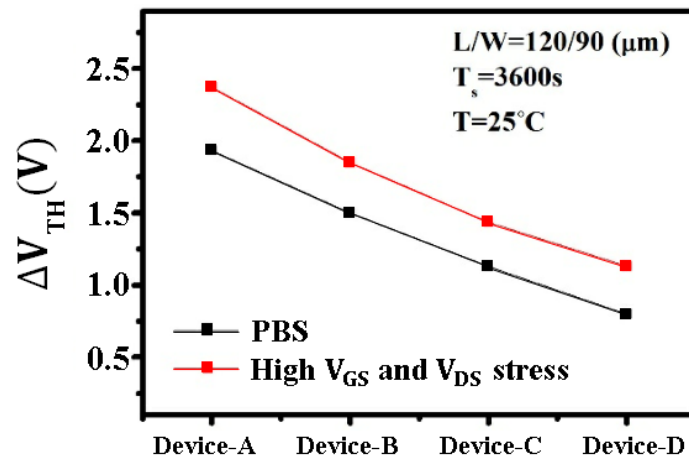

Figure 9. Comparisons of ΔV_{TH} under PBS and high V_{GS} and V_{DS}.

As an explanation of observed results, the concurrent device degradation mechanism in a-IGZO TFTs under high V_{GS} and V_{DS} stress is suggested as a schematic diagram in Figure 10. In the high V_{GS} and V_{DS} stress configuration, in addition to the hot electron-induced degradation near the drain,

the application of a high V_{GS} introduces a PBS component between the gate and the source terminal. Therefore, the cold electrons are injected into the gate insulator and some electrons are trapped into the bulk traps. As reported, some donor-like states can be generated near the source side [28]. At the drain side $V_{GS} = V_{DS}$, the hot electrons can generate the acceptor-like and/or donor-like states (Vo^{2+}), and some hot electrons are injected into the gate insulator. The PBS-induced degradation between the gate and the source reaches its maximum over the source and decreases when moving away along the channel. Consequently, the more severe degradation under high V_{GS} and V_{DS} stress than under PBS is attributed to the device degradation's simultaneous occurrence of due to the cold electrons at the source side and the hot electrons at the drain side.
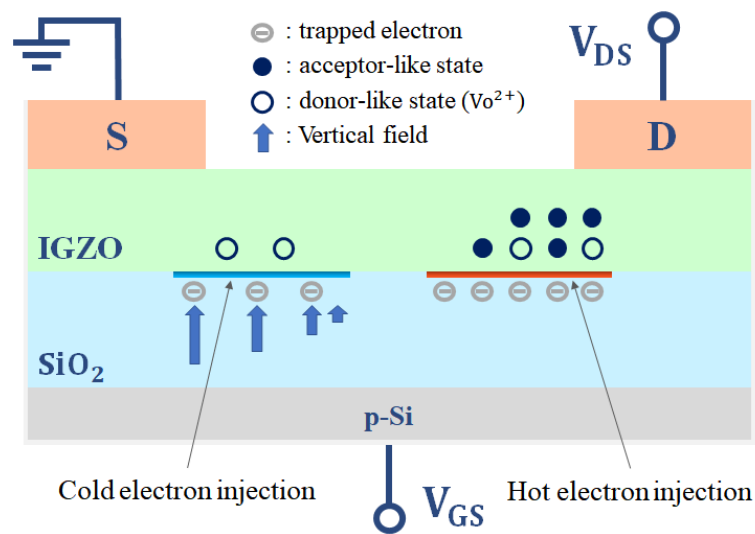

Figure 10. Schematic diagram of the concurrent device degradation mechanism in a-IGZO TFTs under high V_{GS} and V_{DS} stress.

The enhanced performances of the engineered active layer device can be attributed to the fewer grain binaries due to the reduced surface roughness with the increase of In and Zn ratio. The In and Zn rich front layer which has an amorphous structure increases the effective barrier height under PBS. The Ga rich back layer which suppresses the oxygen vacancy passivates a secondary-active channel region. Therefore, the combination mechanism of the passivation and the higher effective barrier heigh treduces the instability in engineered active layer devices. The more significant device degradation under high V_{GS} and V_{DS} stress than under PBS is attributed to the simultaneous occurrence of the device degradation at both the source and drain side.

4. Conclusion

The device performances and the instabilities have been enhanced in engineeredactive layer a-IGZO TFTs due to the high conductive channel's combination with the front In rich layer and the passivation effects with the back Ga rich layer. Considering the device degradation, the In and Zn rich layer for the front primary channel decreases the total trap density and increases the effective barrier height. The Ga rich layer for the back secondary channel can play a role of the passivation

because it suppresses the oxygen vacancy and leads to the decrease of the electron concentration. To explain the more severe device degradation under high V_{GS} and V_{DS} stress than under PBS, the concurrent device degradation mechanism is suggested.

Acknowledgements

Conflict of interests

All authors declare no conflicts of interest in this paper.

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