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Research article

Finite state machine and Markovian equivalents of the *lac* Operon in *E. coli* bacterium

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Abstract: The *lac* operon in *E. coli* has been extensively studied by computational biologists. The bacterium uses it to survive in the absence of glucose, utilizing lactose for growth. This paper presents a novel modeling mechanism for the *lac* operon, transferring the process of lactose metabolism from the cell to a finite state machine (FSM). This FSM is implemented in field-programmable gate array (FPGA) and simulations are run in random conditions. A Markov chain is also proposed for the *lac* operon, which helps study its behavior in terms of probabilistic variables, validating the finite state machine at the same time. This work is focused towards conversion of biological processes into computing machines.

Keywords: digital modeling; *lac* operon; bistable switch; finite state machine; Markov model

Appendix A.

A. Truth table for *Lac* module

The operation of **Lac** module, depicted in Figure 5, is dictated by an extensive truth table. This appendix provides the complete truth table for the 19−state FSM implemented in **DLO**.

The first three columns of Table 1 identify the initial state of the machine, as State Name (from Table 1) and as the actual state code in binary.

The **DLO** module's internal memory is a 3−bit register called **mem**. The fourth column depicts the contents of **mem** before transition of the machine.

Inputs *R* and *C* show the presence of *lac* repressor and CAP, respectively. Other inputs include the *f* bit pair, the *loc* bit pair and the *sel* bit, all generated from a linear-feedback shift register.

It is not necessary that a transition alters the memory **mem**. Hence, memory contents are displayed with revised values only for transitions that modify **mem**. Empty entries in **mem** signify that the relevant bits retain previous values.

Output bit pair *out* is generated with each transition of the machine. The resultant state is indicated in the last column.

Table 1. Truth table for *DLO*.

Initial State			mem			R	C	f	loc	sel	mem			out	Next State
		4 3 2 1 0	2	1	0			1 0	1 0		2	1	0	1 0	←bit subscripts
×	×	×××××	×	×	×	×	×	××	××	×	0	0	0	00	eee
l_0	eee	00000	0	×	×	0	0	××	××	×				00	epe
		00000	1	×	×	0	0	××	××	×	0	0	0	00	eee
		00000	×	×	×	0	1	××	×0	×				00	cee
		00000	×	×	×	0	1	××	×1	×				00	eec
		00000	0	×	×	1	0	00	00	×				00	ree
		00000	0	×	×	1	0	00	01	×				00	eer
		00000	0	×	×	1	0	00	1×	×	1	0	0	00	eee
		00000	0	×	×	1	0	01	××	×	1	0	1	00	ree
		00000	0	×	×	1	0	10	××	×	1	1	0	00	eer
		00000	0	×	×	1	0	11	××	×				00	fef
		00000	1	×	×	1	0	××	×0	×				00	ree
		00000	1	×	×	1	0	××	×1	×				00	eer
		00000	×	×	×	1	1	××	××	×				00	epe
l_1	eer	00001	0	×	×	0	0	××	××	×				00	eee
		00001	1	0	0	0	0	××	×0	×				00	eee
		00001	1	0	0	0	0	××	×1	×	0	0	0	00	eer
		00001	1	1	0	0	0	××	××	×	0	0	0	00	eee
		00001	×	×	×	0	1	××	××	×				00	cer
		00001	0	×	×	1	0	×0	×0	×				00	rer
		00001	0	×	×	1	0	×0	×1	×	1	0	0	00	eer
		00001	0	×	×	1	0	×1	××	×	1	0	1	00	rer
		00001	1	×	×	1	0	××	××	×				00	rer
		00001	×	×	×	1	1	××	××	×				00	epr
l_2	eec	00011	0	×	×	0	0	××	××	×				00	eee
		00011	1	×	×	0	0	××	××	0	0	0	0	00	eec
		00011	1	×	×	0	0	××	××	1				00	eee
		00011	×	×	×	0	1	××	××	×				00	cec
		00011	0	×	×	1	0	×0	×0	×				00	rec
		00011	0	×	×	1	0	×0	×1	×	1	0	0	00	eec
		00011	0	×	×	1	0	×1	××	×	1	0	1	00	rec
		00011	1	×	×	1	0	××	××	×				00	rec
		00011	×	×	×	1	1	××	××	×				00	epc

× implies the input is ignored.

Table 1. Truth table (continued).

Initial State			mem	R	C	f	loc	sel	mem	out	Next State
		4 3 2 1 0	2 1 0			1 0	1 0		2 1 0	1 0	←bit subscripts
l_3	epe	00110	0 × ×	0	0	××	××	×		01	eee
		00110	1 × ×	0	0	××	××	×	0 0 0	00	epe
		00110	× × ×	0	1	××	×0	×		00	cpe
		00110	× × ×	0	1	××	×1	×		00	epc
		00110	0 × ×	1	0	00	00	×		00	rpe
		00110	0 × ×	1	0	00	01	×		00	epr
		00110	0 × ×	1	0	00	1×	×	1 0 0	00	epe
		00110	0 × ×	1	0	01	××	×	1 0 1	00	rpe
		00110	0 × ×	1	0	10	××	×	1 1 0	00	epr
		00110	0 × ×	1	0	11	×0	×		00	rpe
		00110	0 × ×	1	0	11	×1	×		00	epr
		00110	1 × ×	1	0	××	×0	×		00	rpe
		00110	1 × ×	1	0	××	×1	×		00	epr
		00110	× × ×	1	1	××	××	×		01	eee
l_4	epr	01001	0 × ×	0	0	××	××	×		00	epe
		01001	1 0 0	0	0	××	×0	×		00	epe
		01001	1 0 0	0	0	××	×1	×	0 0 0	00	epr
		01001	1 1 0	0	0	××	××	×	0 0 0	00	epe
		01001	× × ×	0	1	××	××	×		00	cpr
		01001	0 × ×	1	0	×0	×0	×		00	rpr
		01001	0 × ×	1	0	×0	×1	×	1 0 0	00	epr
		01001	0 × ×	1	0	×1	××	×	1 0 1	00	rpr
		01001	1 × ×	1	0	××	××	×		00	rpr
		01001	× × ×	1	1	××	××	×		00	eer
l_5	epc	01101	0 × ×	0	0	××	××	×		00	epe
		01101	1 × ×	0	0	××	××	0	0 0 0	00	epc
		01101	1 × ×	0	0	××	××	1		00	epe
		01101	× × ×	0	1	××	××	×		00	cpc
		01101	0 × ×	1	0	×0	×0	×		00	rpc
		01101	0 × ×	1	0	×0	×1	×	1 0 0	00	epc
		01101	0 × ×	1	0	×1	××	×	1 0 1	00	rpc
		01101	1 × ×	1	0	××	××	×		00	rpc
		01101	× × ×	1	1	××	××	×		10	eec

× implies the input is ignored.

Table 1. Truth table (continued).

Initial State			mem			R	C	f	loc	sel	mem			out	Next State
		4 3 2 1 0	2	1	0			1 0	1 0		2	1	0	1 0	←bit subscripts
l_6	ree	00010	0	×	×	0	0	××	××	×				00	eee
		00010	1	0	0	0	0	××	×0	×				00	eee
		00010	1	0	0	0	0	××	×1	×	0	0	0	00	ree
		00010	1	1	0	0	0	××	××	×	0	0	0	00	eee
		00010	×	×	×	0	1	××	××	×				00	rec
		00010	0	×	×	1	0	×0	×0	×				00	rer
		00010	0	×	×	1	0	×0	×1	×	1	0	0	00	ree
		00010	0	×	×	1	0	×1	××	×	1	1	0	00	rer
		00010	1	×	×	1	0	××	××	×				00	rer
		00010	×	×	×	1	1	××	××	×				00	rpe
l_7	rer	00111	0	×	×	0	×	××	×0	×				00	eer
		00111	0	×	×	0	×	××	×1	×				00	ree
		00111	1	0	0	0	×	××	00	×				00	eer
		00111	1	0	0	0	×	××	01	×				00	ree
		00111	1	0	0	0	×	××	1×	×	0	0	0	00	rer
		00111	1	0	1	0	×	××	×0	×	0	0	0	00	eer
		00111	1	0	1	0	×	××	×1	×				00	ree
		00111	1	1	0	0	×	××	×0	×				00	eer
		00111	1	1	0	0	×	××	×1	×	0	0	0	00	ree
		00111	0	×	×	1	×	××	××	×	1	0	0	00	rer
		00111	1	×	×	1	×	××	××	×				00	rpr
l_8	rec	01010	0	×	×	0	0	××	××	0				00	eec
		01010	1	0	0	0	0	××	×0	0				00	eec
		01010	1	0	0	0	0	××	×1	0	0	0	0	00	rec
		01010	1	0	1	0	0	××	××	0	0	0	0	00	eec
		01010	×	×	×	0	0	××	××	1				00	ree
		01010	×	×	×	0	1	××	××	×				00	rpc
		01010	0	×	×	1	0	××	××	×	1	0	0	00	rec
		01010	1	×	×	1	0	××	××	×				00	rpc
		01010	×	×	×	1	1	××	××	×				00	rpc

× implies the input is ignored.

Table 1. Truth table (continued).

Initial State			mem			R	C	f	loc	sel	mem			out	Next State
		4 3 2 1 0	2	1	0			1 0	1 0		2	1	0	1 0	←bit subscripts
l_9	rpe	01011	0	×	×	0	0	××	××	×				00	epe
		01011	1	0	0	0	0	××	×0	×				00	epe
		01011	1	0	0	0	0	××	×1	×	0	0	0	00	rpe
		01011	1	0	1	0	0	××	××	×	0	0	0	00	epe
		01011	×	×	×	0	1	××	××	×				00	rpc
		01011	0	×	×	1	0	×0	×0	×				00	rpr
		01011	0	×	×	1	0	×0	×1	×	1	0	0	00	rpe
		01011	0	×	×	1	0	×1	××	×	1	1	0	00	rpr
		01011	1	×	×	1	0	××	××	×				00	rpr
		01011	×	×	×	1	1	××	××	×				01	ree
l_{10}	rpr	01111	0	×	×	0	×	××	×0	×				00	epr
		01111	0	×	×	0	×	××	×1	×				00	rpe
		01111	1	0	0	0	×	××	00	×				00	epr
		01111	1	0	0	0	×	××	01	×				00	rpe
		01111	1	0	0	0	×	××	1×	×	0	0	0	00	rpr
		01111	1	0	1	0	×	××	×0	×	0	0	0	00	epr
		01111	1	0	1	0	×	××	×1	×				00	rpe
		01111	1	1	0	0	×	××	×0	×				00	epr
		01111	1	1	0	0	×	××	×1	×	0	0	0	00	rpe
		01111	0	×	×	1	×	××	××	×	1	0	0	00	rpr
		01111	1	×	×	1	×	××	××	×				00	rer
l_{11}	rpc	10001	0	×	×	0	0	××	××	0				00	epc
		10001	1	0	0	0	0	××	×0	0				00	epc
		10001	1	0	0	0	0	××	×1	0	0	0	0	00	rpc
		10001	1	0	1	0	0	××	××	0	0	0	0	00	epc
		10001	×	×	×	0	0	××	××	1				00	rpe
		10001	×	×	×	0	1	××	××	×				10	rec
		10001	0	×	×	1	0	××	××	×	1	0	0	00	rpc
		10001	1	×	×	1	0	××	××	×				10	rec
		10001	×	×	×	1	1	××	××	×				10	rec
l_{12}	cee	00100	0	×	×	0	0	××	××	×				00	eee
		00100	1	×	×	0	0	××	××	0	0	0	0	00	cee
		00100	1	×	×	0	0	××	××	1				00	eee
		00100	×	×	×	0	1	××	××	×				00	cec
		00100	0	×	×	1	0	×0	×0	×				00	cer
		00100	0	×	×	1	0	×0	×1	×	1	0	0	00	cee
		00100	0	×	×	1	0	×1	××	×	1	1	0	00	cer
		00100	1	×	×	1	0	××	××	×				00	cer
		00100	×	×	×	1	1	××	××	×				00	cpe

× implies the input is ignored.

Table 1. Truth table (continued).

Initial State			mem	R	C	f	loc	sel	mem	out	Next State
		4 3 2 1 0	2 1 0			1 0	1 0		2 1 0	1 0	←bit subscripts
l_{13}	cer	01000	0 × ×	0	0	××	××	0		00	cee
		01000	0 × ×	0	0	××	××	1		00	eer
		01000	1 0 0	0	0	××	×0	0		00	cee
		01000	1 0 0	0	0	××	×1	0	0 0 0	00	cer
		01000	1 1 0	0	0	××	××	0	0 0 0	00	cee
		01000	1 1 0	0	0	××	××	1		00	eer
		01000	× × ×	0	1	××	××	×		00	cpr
		01000	0 × ×	1	0	××	××	×	1 0 0	00	cer
		01000	1 × ×	1	0	××	××	×		00	cpr
		01000	× × ×	1	1	××	××	×		00	cpr
l_{14}	cec	01100	0 × ×	0	0	××	×0	×		00	eec
		01100	0 × ×	0	0	××	×1	×		00	cee
		01100	1 × ×	0	0	××	××	0	0 0 0	00	cec
		01100	1 × ×	0	0	××	×0	1		00	eec
		01100	1 × ×	0	0	××	×1	1		00	cee
		01100	× × ×	0	1	××	××	×		00	cpc
		01100	0 × ×	1	0	××	××	×	1 0 0	00	cec
		01100	1 × ×	1	0	××	××	×		00	cpc
		01100	× × ×	1	1	××	××	×		00	cpc
l_{15}	cpe	01110	0 × ×	0	0	××	××	×		00	epe
		01110	1 × ×	0	0	××	××	0	0 0 0	00	cpe
		01110	1 × ×	0	0	××	××	1		00	epe
		01110	× × ×	0	1	××	××	×		00	cpc
		01110	0 × ×	1	0	×0	×0	×		00	cpr
		01110	0 × ×	1	0	×0	×1	×	1 0 0	00	cpe
		01110	0 × ×	1	0	×1	××	×	1 1 0	00	cpr
		01110	1 × ×	1	0	××	××	×		00	cpr
		01110	× × ×	1	1	××	××	×		10	cee
l_{16}	cpr	10000	0 × ×	0	0	××	××	0		00	cpe
		10000	0 × ×	0	0	××	××	1		00	epr
		10000	1 0 0	0	0	××	×0	0		00	cpe
		10000	1 0 0	0	0	××	×1	0	0 0 0	00	cpr
		10000	1 0 0	0	0	××	××	1		00	epr
		10000	1 0 1	0	0	××	××	0	0 0 0	00	cpe
		10000	1 0 1	0	0	××	××	1		00	epr
		10000	× × ×	0	1	××	××	×		00	cer
		10000	0 × ×	1	0	××	××	×	1 0 0	00	cpr
		10000	1 × ×	1	0	××	××	×		00	cer
		10000	× × ×	1	1	××	××	×		00	cer

× implies the input is ignored.

Table 1. Truth table (continued).

Initial State			mem			R	C	f	loc	sel	mem			out	Next State
		4 3 2 1 0	2	1	0			1 0	1 0		2	1	0	1 0	←bit subscripts
l_{17}	cpc	10010	0	×	×	0	0	××	×0	×				00	epc
		10010	0	×	×	0	0	××	×1	×				00	cpe
		10010	1	×	×	0	0	××	××	0	0	0	0	00	cpc
		10010	1	×	×	0	0	××	×0	1				00	epc
		10010	1	×	×	0	0	××	×1	1				00	cpe
		10010	×	×	×	0	1	××	××	×				11	cec
		10010	0	×	×	1	0	××	××	×	1	0	0	00	cpc
		10010	1	×	×	1	0	××	××	×				11	cec
		10010	×	×	×	1	1	××	××	×				11	cec
l_{18}	fef	00101	0	×	×	0	×	××	××	×				00	eee
		00101	1	×	×	0	×	××	×0	×				00	eee
		00101	1	×	×	0	×	××	×1	×	0	0	0	00	fef
		00101	0	×	×	1	×	××	××	×	1	0	0	00	fef
		00101	1	×	×	1	×	××	××	×				00	fef

× implies the input is ignored.